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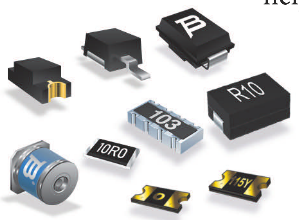

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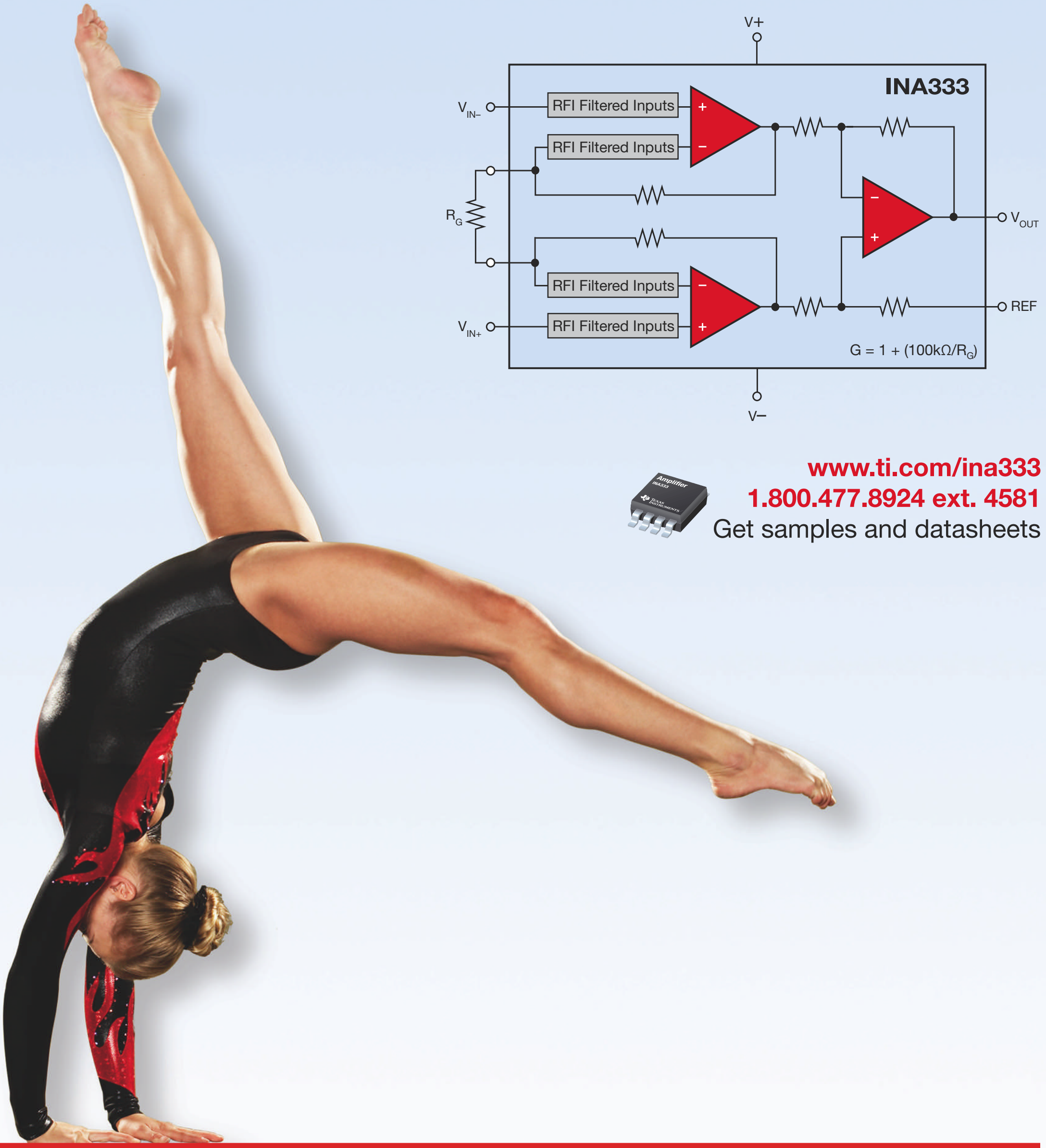
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R_G
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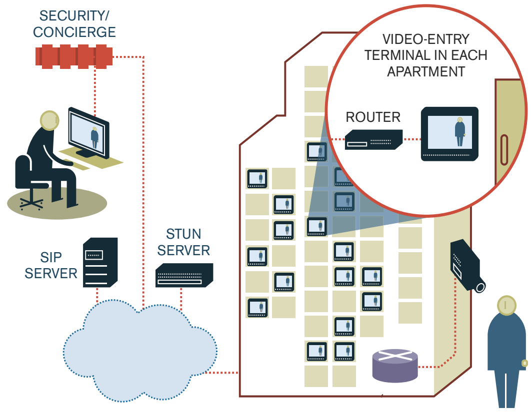
3G wireless data: about to break?

40 Although the definitions of 3 and 4G wireless data networks, services, and terminals have been moving targets, some long-promised 3G capabilities are starting to appear. Meanwhile, 4G deployments have been delayed even further. *by Ann R Thryft, Contributing Editor*

Solid-state drives challenge hard disks

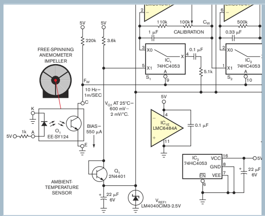
25 Hard-disk-drive vendors assert that more-than-50-year-old rotating storage will remain relevant for many years to come. Solid-state-drive suppliers scoff at these claims, calling hard-disk technology a has-been. Which camp is right? *by Brian Dipert, Senior Technical Editor*



Designing intelligence into door-entry and security systems

51 Designers now have greater opportunity than ever before to design more intelligence and flexibility into personal-security systems by using mature and proven standards-based technology. Learn about some of the key challenges to implementing high-quality, cost-effective, and secure door-entry and video-monitoring systems using IP voice and video technology. *by Gordon Wilkinson, PhD, Trinity Convergence*

DESIGNIDEAS



61 Linear wind-power meter compensates for temperature
62 Oscillator uses dual-output current-controlled conveyors
64 Circuits drive single-coil latching relays

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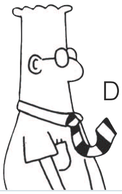

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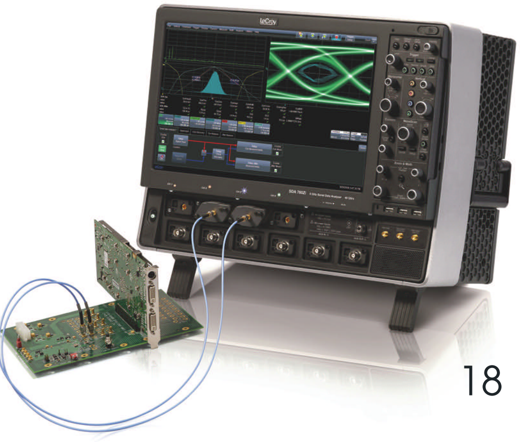
17 New approach to ink boosts solar-cell efficiency to more than 17%

17 Piccolo processors focus on real-time control for cost-sensitive designs

18 High-performance scopes enhance serial-data analysis

20 **Research Update:** Energy scavenger achieves record power; Researchers explore nonvolatile resistive RAM as flash replacement



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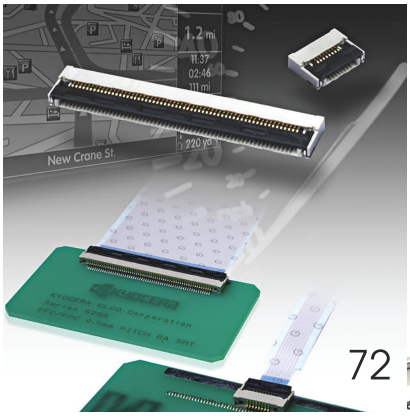

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PRODUCT ROUNDUP

72 **Connectors:** ZIF-connector series, end-to-end cabling devices, audio connectors, and interface devices

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Networked Motors: 40MHz 16-bit Timers and LIN/CAN Modules

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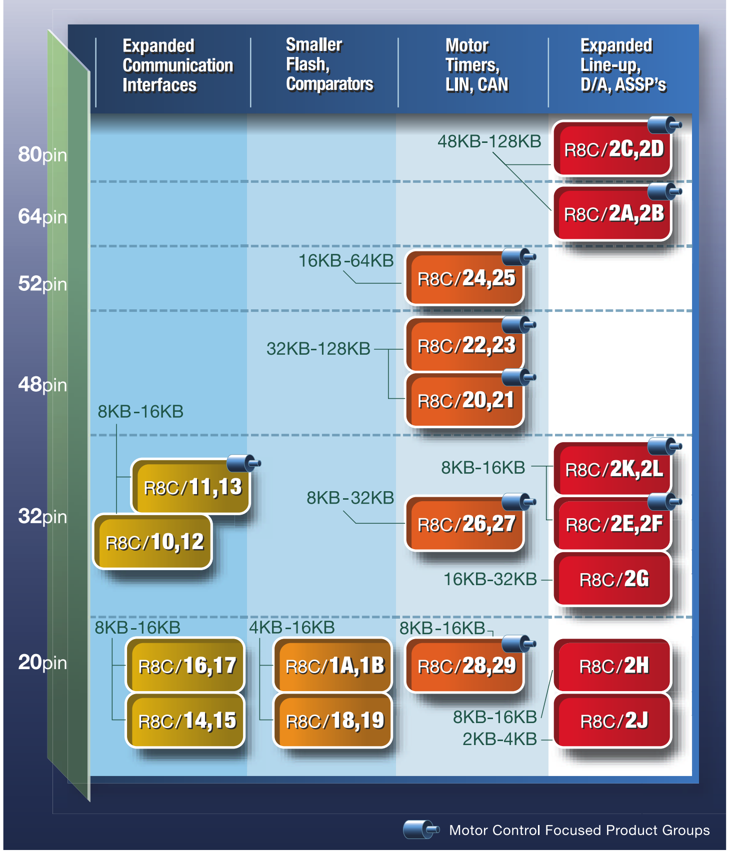
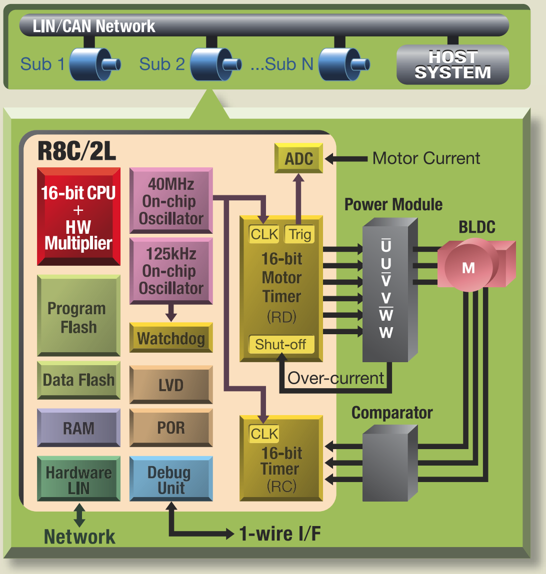
R8C/Tiny Product Lineup



HOT Products **R8C/2L**

Ideal for Networked BLDC Motor systems



Top Reasons For Selecting R8C/Tiny's Motor Control Solutions

- **High-Performance**
  - 16-bit CPU core with hardware multiplier
  - Up to three 16-bit timers with 40MHz clock
  - 3.3µs ADC conversion with timer-trigger start option
- **Advanced Motor-Tuned Timers**
  - Up to 6-ch complementary PWM signals with independent compare registers
  - Programmable Dead-Time Control (16-bit)
  - Selectable buffer operation for fast timer reload
  - PWM signal shut-off using external trigger
- **High Component Integration**
  - Integrated LIN and CAN modules for networking
  - Watchdog with dedicated On-chip Oscillator
  - Power-on Reset, Voltage Detection Circuits and Data Flash
- **Outstanding Development Support**
  - Multiple motor control algorithms
  - Demonstration and reference design platforms

*Source: Gartner "Semiconductor Applications Worldwide Annual Market Share: Database" Hiroyuki Shimizu, 27 March 2008, GJ08218 ＊This is 2007 ranking

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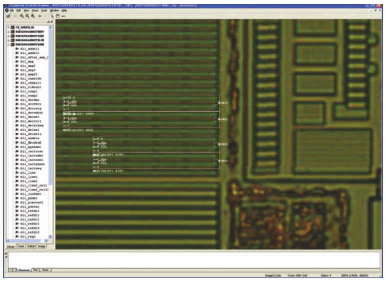

ONLINE ONLY

Check out these Web-exclusive articles:

DDR3 SDRAM exposed: inside a bleeding-edge, blazing-fast memory device
The IC Insider reveals the densely packed real estate and impressive clock-synchronization circuitry that allow Samsung's 1-Gbit K4B1G0846D-HCF8 to achieve its 1066-Mbps data-transfer rate.
→www.edn.com/article/CA6609129

Designing very-high-frequency signal generators with amplifier ICs
→www.edn.com/article/CA6604951

A new way to handle RF/PCB design
→www.edn.com/article/CA6608071

IMEC describes energy, memory initiatives, announces processor licensing
→www.edn.com/article/CA6606807

POE devices cater to higher-powered applications
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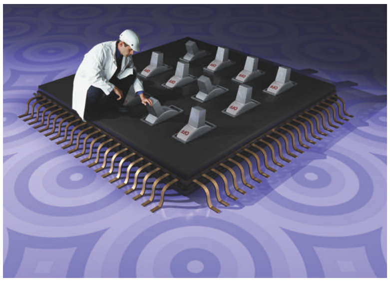

READERS' CHOICE

A selection of recent articles receiving high traffic on www.edn.com.

A turn-off: Power management complicates life for verification engineers
Advanced energy-saving techniques can cause vast difficulties in the verification process.
→www.edn.com/article/CA6602444

Mutliplexing technique yields a reduced-pin-count LED display
→www.edn.com/article/CA6602447

Re-engineering obsolete ICs using FPGAs
→www.edn.com/article/CA6604712

IBM extends China research
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Power-over-Ethernet chips: to the spec and beyond
→www.edn.com/article/CA6602445

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An *EDN* contributor since the early 1980s, Linear Technology's Jim Williams consistently turns out technical articles that rank near the top of our Readers' Choice lists. Check out the new online archive of Williams' articles.
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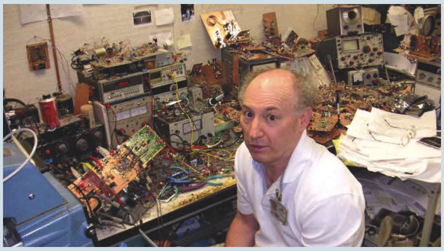

EDN INNOVATION

NOMINATION DEADLINE APPROACHES

Get your nominations in by Nov 26 for *EDN*'s 19th annual Innovation Awards, which will take place in March 2009. Visit the Innovation home page to learn about and begin the simple nomination process.
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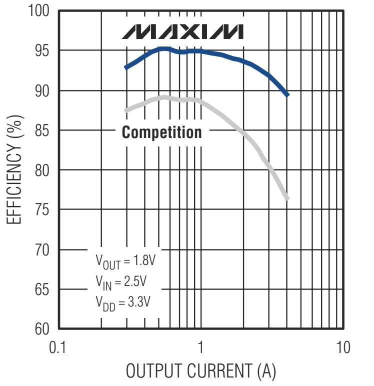
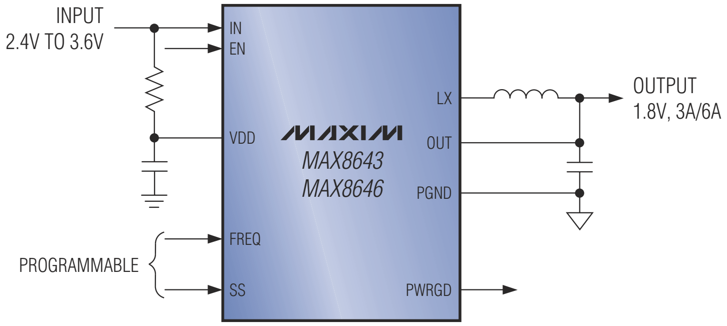
Buck regulators with integrated MOSFETs simplify designs up to 25A/phase

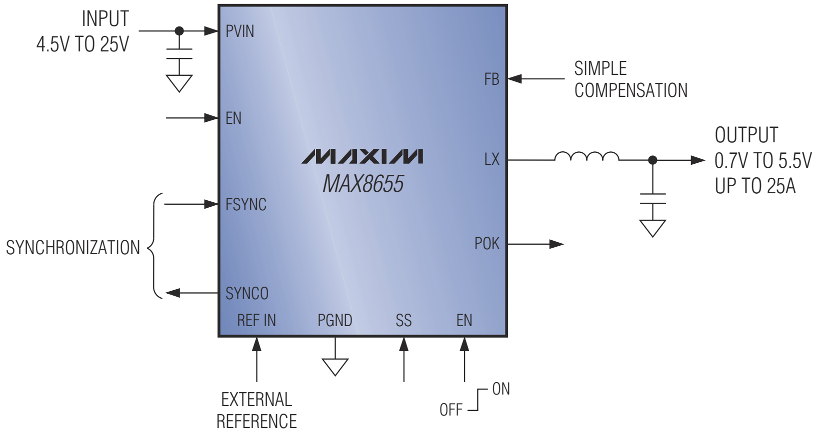
High efficiency

EFFICIENCY VS. OUTPUT CURRENT





High output current



Feature	MAX8655	Competition
Output current (A)	25	12
Input voltage (V)	4.5 to 25	4 to 24
Package (mm x mm)	8 x 8	9 x 9

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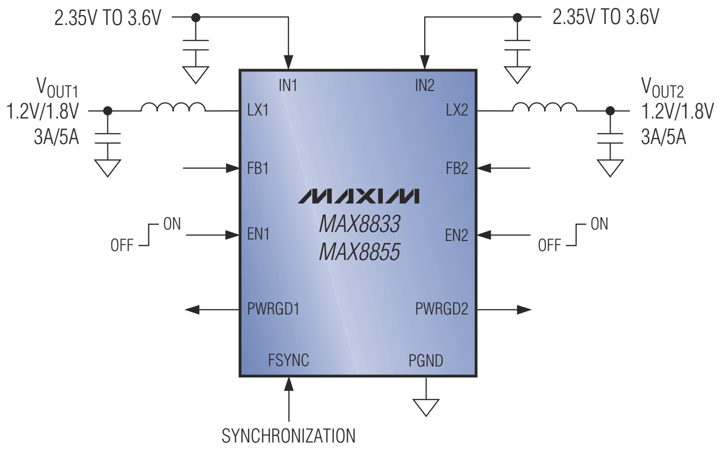
- **Tracking/sequencing**
- **All-ceramic capacitor design**
- **180° out-of-phase operation reduces input ripple**
- **5mm x 5mm, 32-pin TQFN package**



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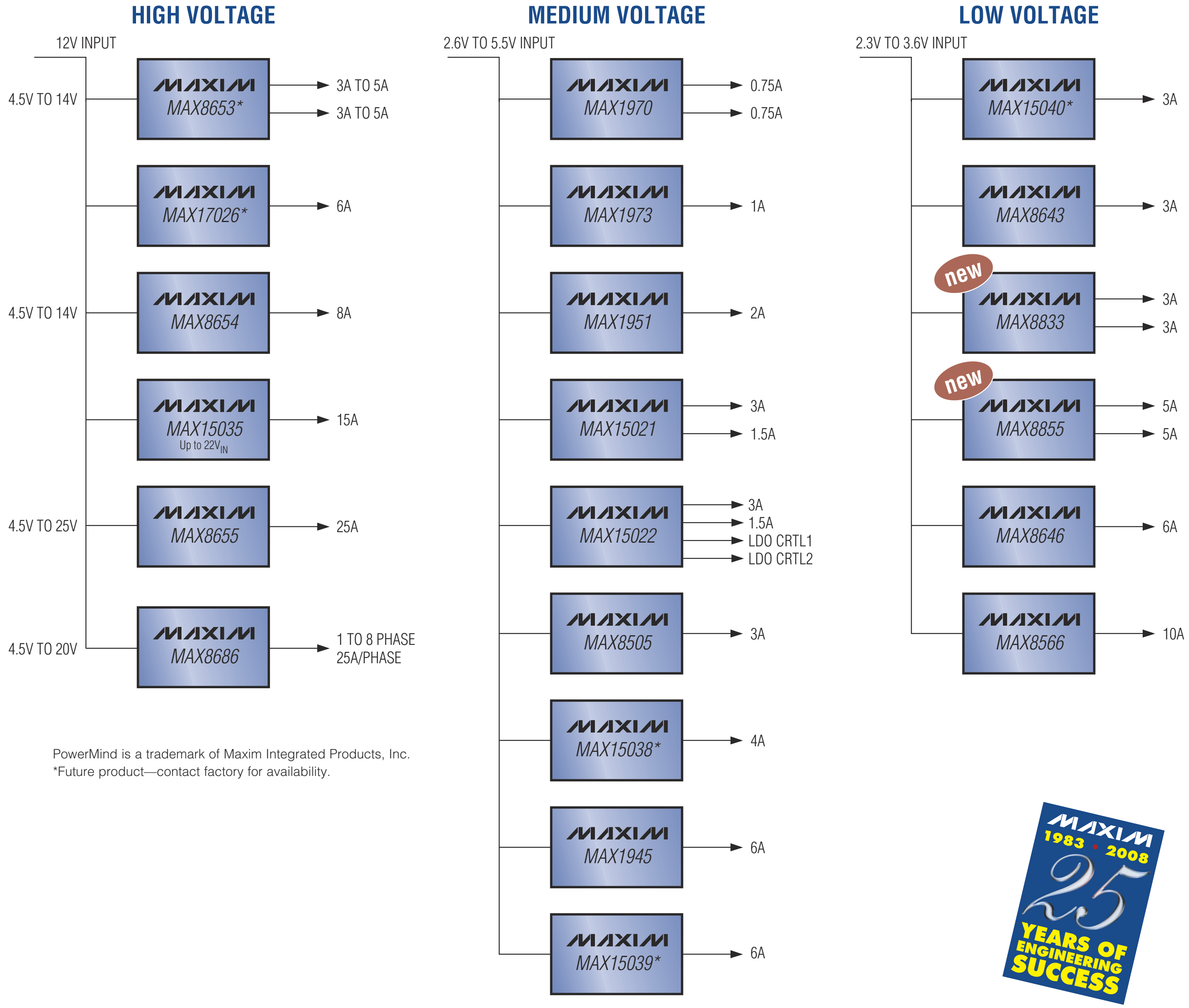

HIGH VOLTAGE

12V INPUT

- 4.5V TO 14V: MAX8653* → 3A TO 5A, 3A TO 5A
- MAX17026* → 6A
- 4.5V TO 14V: MAX8654 → 8A
- MAX15035 (Up to $22V_{IN}$) → 15A
- 4.5V TO 25V: MAX8655 → 25A
- 4.5V TO 20V: MAX8686 → 1 TO 8 PHASE 25A/PHASE

MEDIUM VOLTAGE

2.6V TO 5.5V INPUT

- MAX1970 → 0.75A, 0.75A
- MAX1973 → 1A
- MAX1951 → 2A
- MAX15021 → 3A, 1.5A
- MAX15022 → 3A, 1.5A, LDO CRTL1, LDO CRTL2
- MAX8505 → 3A
- MAX15038* → 4A
- MAX1945 → 6A
- MAX15039* → 6A

LOW VOLTAGE

2.3V TO 3.6V INPUT

- MAX15040* → 3A
- MAX8643 → 3A
- new MAX8833 → 3A, 3A
- new MAX8855 → 5A, 5A
- MAX8646 → 6A
- MAX8566 → 10A

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BY RICK NELSON, EDITOR-IN-CHIEF

Tech innovation addresses societal, environmental challenges worldwide

Intensive research and development in nanoelectronics and nanotechnology is critical for tackling societal and environmental challenges facing the world today. Speaking at the IMEC (www.imec.be) ARRM (Annual Research Review Meeting) on Oct 13, in Leuven, Belgium, Luc Van den hove, executive vice president and chief operating officer at IMEC, outlined several areas of concentration that the independent research center is addressing in conjunction with its partners. Two major areas, he said, are health care and energy.

Health care is particularly ripe for innovations that can provide increased levels of care at lower costs. Today, Van den hove said, blood analysis is a labor-intensive process that can take a couple of days. In the future, he added, a "lab on a chip" will be able to promptly, accurately, and inexpensively provide results. Going further, he said, in-body and wearable sensors—powered by energy-harvesting techniques—will provide early warnings of potential health problems.

In separate presentations, IMEC personnel said that the organization should be well-positioned to address health-care issues. Kris Verstreken, program director of biomedical electronics, said the cell is the most complex MEMS (microelectromechanical) device you can imagine, combining electrical, chemical, and mechanical functions in a nanoscale dynamic environment. IMEC's nanotechnology, he added, operates at the same scale and paves the way for various health-related applications, including deep-brain stimulation for treatment of Parkinson's disease, epilepsy, and obsessive-compulsive disorder, as well as metal nanoparticle hyperthermia for cancer treatment.

> **Health care is particularly ripe for innovations that can provide increased levels of care at lower costs.**

Bert Gyselinckx, program director for wireless-autonomous-transducer solutions at IMEC, demonstrated an emotion-monitoring body-area network system that could have applications in reducing stress and increasing task engagement. Carmen Bartic, who coordinates the research activities of the Bioelectronic Systems Group at IMEC, described cell-to-electronics interfaces that could result in implantable probes that combine stimulus and recording capabilities, and Chris Van Hoof, program director for integrated systems and smart implants, provided detail on implantable neuroprobes.

As for energy, Van den hove noted that the sun provides 165,000 TW of free solar power. Researchers need only to find a way to capture, store, and transform solar energy in an environmentally friendly manner. As an approach to solving the problem, he cited thin-wafer silicon solar cells that enable such innovations—from IMEC spin-off Photovoltech—as building-integrated solar facades.

Jef Poortmans, director of the solar- and organic-technologies department at IMEC, elaborated on the challenges facing the adoption of solar technology. Today, he said, photovoltaic panels are not competitive without government subsidy. Efforts to wring costs from photovoltaic installations center on minimizing the grams of silicon required per watt-peak, which IMEC is working to accomplish by minimizing wafer loss, reducing active-layer thickness, and increasing efficiencies beyond 20%. Such efforts could help meet European goals of installing 400 GW of peak solar capacity by 2020, accounting for 12% of the continent's energy supply.

Although based in Belgium, IMEC works with partners worldwide to help develop and deploy advanced semiconductor technology. Such cooperative efforts will become increasingly important as technology advances and R&D becomes ever more costly. Particularly in times of economic stress, it makes sense for companies to cooperate on precompetitive research, as IMEC President and Chief Executive Officer Gilbert Declerck suggested during his ARRM presentation.

But that's not to say innovation can't happen on a smaller scale. Published with this issue of *EDN* is *EDN Global Innovators 2008*, which highlights how technological innovation occurs across the gamut of organizational environments—from start-up fabless-semiconductor companies to large automotive manufacturers. Read more at edn.com/global08.**EDN**

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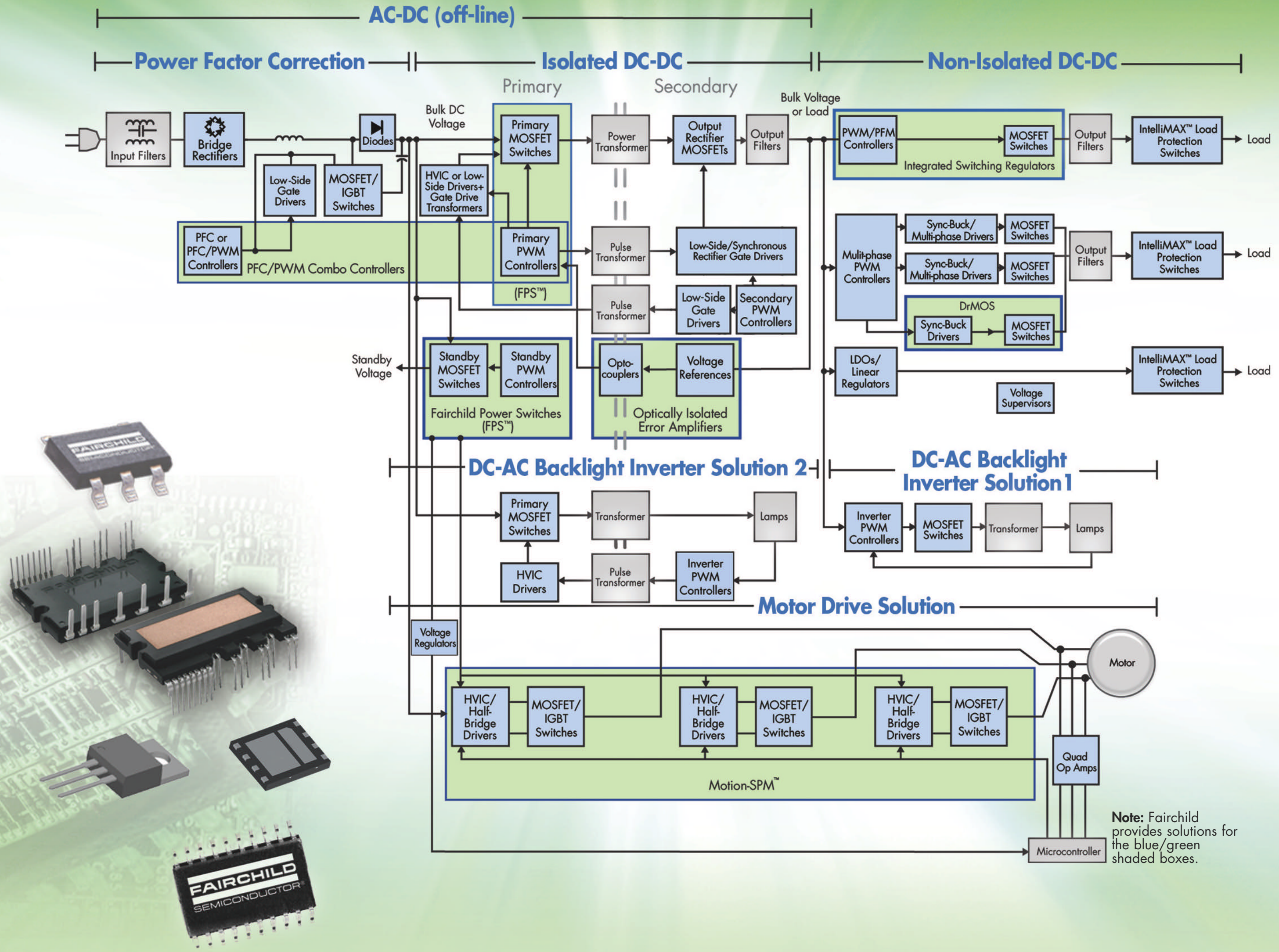

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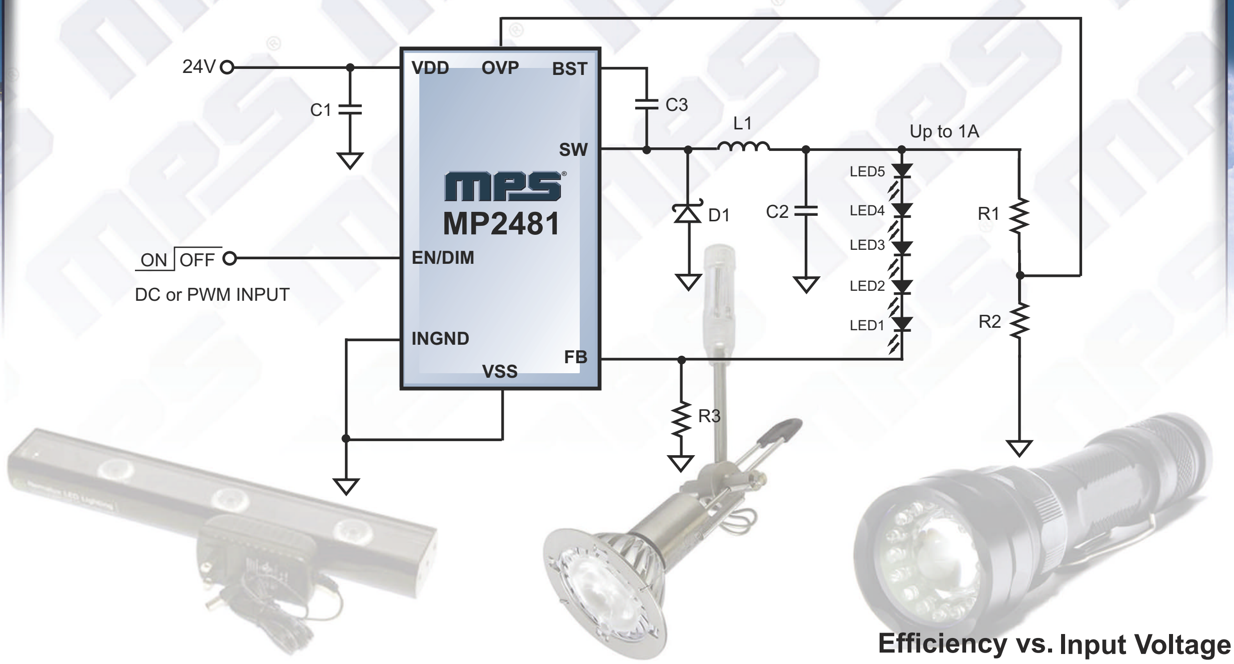
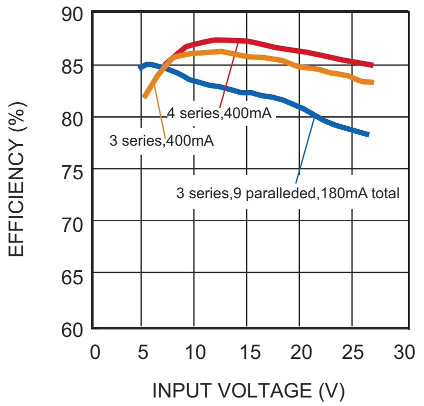


Efficiency vs. Input Voltage

Step-up/down Application



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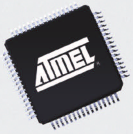

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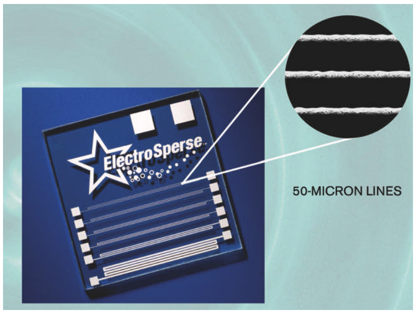
EDITED BY FRAN GRANVILLE

pulse

INNOVATIONS & INNOVATORS

New approach to ink boosts solar-cell efficiency to more than 17%

Advances in solar-cell efficiency usually focus on the cell itself: In a monocrystalline-silicon-solar cell, the efficiency can be as high as 18 or 19%. However, these high figures don't account for the efficiency—or inefficiency—of the collector electrodes, which are screen-printed onto the silicon emitter that forms the top of the solar cell. This surface collects the sunlight and converts it to current. However, today's solar inks suspend within them silver conducting particles and typically achieve line widths of 120 to 175 microns—wide enough to block sunlight and, hence, reduce efficiency. If the lines were any narrower, more surface area of silicon would be exposed to the sun.



Narrower collection lines on the surface of solar cells can increase cell efficiency by as much as 9%.

Five Star Technologies has addressed this problem by using a hydrodynamic-cavitation process instead of a traditional milling process to create the silver particles in its new ElectroSperse S-540 ink. The new technology yields finer, size-controlled silver particles with lines as narrow as 80 to 100 microns in the screen-printing process. The company claims that the technology can enhance solar-panel efficiency by as much as 9% when more and narrower lines contact the panel's silicon emitter. Tests at the Georgia Institute of Technology (www.gatech.edu) revealed cell efficiencies of 17.4% for the monocrystalline cells that Five Star produced with ElectroSperse S-540 ink.

—by Margery Conner

▷**Five Star Technologies**, www.fivestartech.com.

FEEDBACK LOOP

"Though the electronics industry stands to profit from the design and manufacture of white-spaces devices, we shouldn't effectively be shutting out current broadcast-TV viewers under the banner of 'progress.'"

—Reader Dan White, in *EDN*'s Feedback Loop, at www.edn.com/article/CA6602449. Add your comments.

Piccolo processors focus on real-time control for cost-sensitive designs

Texas Instruments' new Piccolo series TMS320F280xx processors integrate a C28x processor core, peripherals, and a CLA (control-law accelerator). The devices target price-sensitive control applications, such as solar-power microinverters, white goods, and LED lighting, that benefit from advanced control algorithms. This series of processors is available for prices as low as $2 each (high volumes). Devices in the Piccolo F2803x series feature a programmable CLA that enables developers to offload control algorithms from the main processor. The CLA includes an independent, 32-bit, floating-point-math accelerator.

On-chip ePWMs (enhanced pulse-width modulators) support a frequency modulation as low as 150 psec. To reduce system BOM (bill-of-materials) costs, these devices include two on-chip oscillators that operate at 10 MHz with ±1% accuracy. Integrated oscillators feature triple redundancy and on-chip self-test for compliance with system-level safety certification, such as the IEC 60730 safety standard that European white goods require. The power architecture enables designers to use a 3.3V supply with an internal regulator at voltages as low as 1.9V to provide brown-out protection and power-on-reset support.

The initial devices support operating speeds of 40 and 60 MHz with as much as 128 kbytes of flash memory, a 12-bit ADC, an ePWM, on-chip oscillators, analog comparators, and code compatibility with earlier C2000 devices. To support development with these processors, the company plans next month to introduce a $49, F280xxx-microcontroller-based, removable controlCard target board.**—by Robert Cravotta**

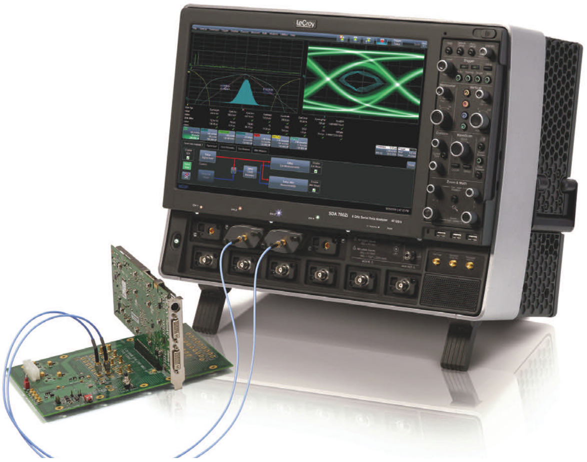
▷**Texas Instruments**, www.ti.com.

High-performance scopes enhance serial-data analysis

LeCroy has introduced the SDA 7 Zi oscilloscopes with built-in SDA (serial-data-analysis) II serial-data-debugging software, which the manufacturer says redefines SDA in oscilloscopes. The new scopes go beyond compliance testing and introduce five debugging approaches that visually predict BER (bit-error rate) directly on the eye diagram; provide two methods of decomposing jitter, displaying them both numerically and with insightful graphics; provide a Quick-View feature as part of an intuitive eye- and jitter-breakdown master display; measure millions of unit intervals at speeds as high as 50 times those of other scopes; and integrate both compliance testing and SDA II-debugging tools to help you pinpoint the cause of UUT (unit-under-test) malfunctions.

SDA II includes the IsoBER analysis tool, which extrapolates eye-diagram data and displays contours of constant BER directly on the eye. This approach helps to quickly determine the minimum eye opening and detect crosstalk by analyzing the eye's vertical closure. Standard eye-diagram techniques, such as mask testing, do not allow these measurements because such techniques fail to account for vertical noise and jitter.

Because their X-Stream II architecture is as much as 50 times as fast as other scope architectures, the new instruments are the first to be able to analyze jitter by simultaneously calculating the results of two decomposition algorithms. The instruments use both traditional spectral decomposition and normalized Q-scale decomposition to account for situations in which crosstalk or other types of deterministic jitter masquerade as random jitter and produce incorrect results. (Q is a variable that expresses normal probability distributions so that they appear linear instead of gaussian.) A color-coded warning appears when the two results differ, ensuring the display of correct jitter values.


SDA 7 Zi scopes' innovative displays quickly lead to insights into the causes of misbehavior in high-bit-rate serial-data links.

Distinguishing between random and deterministic jitter is a crucial part of identifying and debugging jitter sources. SDA II provides intuitive graphical views of jitter decomposition to provide faster insight into the cause of problems. To understand deterministic-jitter values and their sources, SDA II displays a periodic-jitter spectrum, which identifies the sources that contribute the highest values of periodic jitter; an ISI (intersymbol-interference) plot, which isolates bit patterns that contribute the most ISI; and a DDJ (data-dependent-jitter) histogram for deeper insight into the DDJ distribution.

SDA 7 Zi scopes extend the recently introduced WavePro 7 Zi Series and come with twice the standard memory to capture more unit intervals in the eye diagram. The fastest eye building combines with the largest number of unit intervals per second to yield the shortest time to achieving an understanding of UUT behavior. To take full advantage of the processing speed, a Quick-View display simultaneously shows the eye diagram, spectrum, normalized Q-Scale jitter decomposition, time-interval error, jitter histogram, and bathtub curve. You can easily reconfigure Quick-View to show as many as 35 measurements and six displays on the 15.3-in.-diagonal, 16×9-aspect ratio, high-resolution, touchscreen. Moreover, you can extend the work space by integrating the view with that of an available second display that has similar characteristics.

The SDA 7 Zi features an advanced industrial design whose removable front panel lets you place the control pod next to the UUT. A new serial-interface bus transfers data 10 to 100 times as fast as do older scopes. In addition, the TriggerScan and WaveScan modes for finding rare events shorten the time to debug new designs. SDA 7 Zi US prices for units that take 40G samples/sec/channel and offer capture memory of 20 million points/channel begin at $39,490 for 2.5-GHz-bandwidth units and extend to $69,490 for 6-GHz units. You can add SDA II to existing WavePro 7 Zi scopes for $7995, and you can add SDA II to older SDA scopes for $3995.**—by Dan Strassberg**

▷**LeCroy Corp,** www.lecroy.com.

DILBERT By Scott Adams

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ANALOG DEVICES

RESEARCH UPDATE

BY RON WILSON

Energy scavenger achieves record power

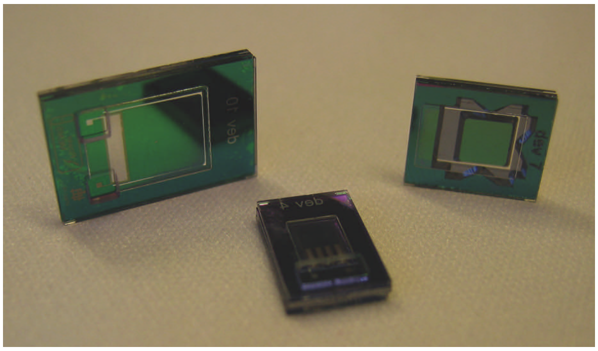
Engineers and scientists have long had an intense interest in energy-scavenging devices that can extract small amounts of electrical energy from such ambient sources as temperature gradients, incident light, stress, or vibration. Such devices can power remote wireless sensors or other low-drain electronic devices in inaccessible locations without the need for periodic battery changes.

Recently, IMEC in Leuven, Belgium, announced a record-breaking power output from such a device: 60 μW—sufficient to power a sensor and a wireless PAN (personal-area-network connection). The previous record was a 40 μW device.

The new record-holder is a piezoelectric-energy harvester. The micromachined design employs a piezoelectric capacitor mounted on a cantilever. The researchers weighted the cantilever at its end to produce a resonant frequency at 500 Hz—well within the range of vibrations most machinery and rotating automobile tires produce. This point raises interesting possibilities for the age of mandatory tire-pressure sensors.

A unique feature of the design is that, instead of choosing the widely used lead-zirconate-titanate film as a piezoelectric material, the researchers selected aluminum nitride. Aluminum nitride is compatible with CMOS processes, making it less expensive to fabricate, and engineers could potentially integrate it onto a monolithic-sensor die, allowing a lower cost for the harvesters.

▷**IMEC**, www.imec.be.



These piezoelectric-energy harvesters set a record in power output: 60 μW.

RESEARCHERS EXPLORE NONVOLATILE RESISTIVE RAM AS FLASH REPLACEMENT

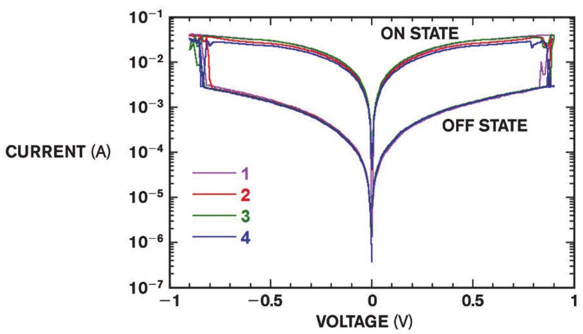
As the end of the road draws ever nearer for flash memory, researchers are leaving no stone unturned in their attempts to find an alternative nonvolatile-storage mechanism that can scale to processes smaller than 32 nm–the point at which, many fear, flash may run out of gas. These explorations have encompassed magnetoresistive RAM, phase-change memory, and a number of other mechanisms. Researchers are, however, still investigating new materials, perhaps indicating the lack of definitive progress in any of the other areas.

IMEC in Leuven, Belgium, recently announced the start of just such a major effort aimed at resistive-RAM technologies employing metal-oxide films. The researchers are not yet committing to a chemistry because the metal stack, a sandwich comprising the top and the bottom electrodes and a film between them, will be one of the primary areas of research.

The area is promising because scientists already know that a metal-oxide film trapped between two electrodes can, in some cases, exhibit a stable, reversible shift in resistance in response to an external voltage. Researchers can then detect the resistance by applying a voltage below the device's switching threshold to the cell and then measuring the current. This approach allows for a simple memory array: a crossbar arrangement in which the intersection of every row and every column is a sandwich with a dot of metal oxide in the middle.

A great deal of engineering must take place between the researchers' demonstration of a stable state change for 1 bit in a laboratory and the production of a large-scale, manufacturable, 22-nm memory with acceptable retention, durability, and speed. IMEC hopes to address all these areas in its program.

▶IMEC, www.imec.be.



Extreme voltage excursions in a resistive-RAM cell cause it to switch between stable higher- and lower-resistance states.

Rarely Asked Questions

Strange stories from the call logs of Analog Devices

Off-Amps, What the Heck Are Off-Amps? Op Amps with No Power Applied, of Course.

Q. What kind of performance (pick a parameter, it could be input impedance or any other op amp specification) can I expect from your amplifier… when the power is off?

A. This may seem like a strange question, but as the title says, "Strange stories from the call logs…" A few times a year we receive questions like this. The specifics vary slightly from customer to customer, but ultimately they want to know how the off-amp will behave in their circuit. A recent customer email asked if the high input impedance of a FET amplifier would be maintained with the power off and a dc voltage at the amplifier input. The short answer was no, but they could maintain a high input impedance over a limited input voltage range by adding a few well placed external diodes.

As you might guess, these questions are not always the easiest or quickest to answer. We don't test any of our amplifiers without power, and I don't know anyone who does. Getting to the bottom of these questions usually requires delving into the inner workings of the off-amp at the transistor level. The circuit configuration, external stimulus, and amplifier type are all factors when it comes to answering questions about off-amps.

The designer is usually seeking advice and guidance on topics such as isolation, input impedance, current limiting, and protecting the off-amp under a variety of conditions. The advice we most often prescribe is to limit the current entering the off-amp. It's surprising how many sneak paths there are within an off-amp. One of the first elements that comes into play is the off-amp's electrostatic discharge (ESD) protection diodes. With an amplifier configured for unity gain, for example, 1 V on the noninverting input is enough to fully turn on an ESD diode. Without current limiting, the diode and even the amplifier can be destroyed. We recommend that current entering an input or output of an off-amp be limited to approximately 5 mA or less. In many cases, a series resistor is all that is needed. At other times, additional components may be required to ensure proper protection of the off-amp.

Next time you come upon an off-amp, remember that limiting the current is paramount, but a fool proof method of protecting an off-amp is to make sure everything else in the circuit is switched off as well!

To Learn More About Op Amp Performance
Go to: http://designnews.hotims.com/22267-101

Contributing Writer John Ardizzoni is an Application Engineer at Analog Devices in the High Speed Linear group. John joined Analog Devices in 2002, he received his BSEE from Merrimack College in N. Andover, MA and has over 28 years experience in the electronics industry.

Have a question involving a perplexing or unusual analog problem? Submit your question to: raq@reedbusiness.com

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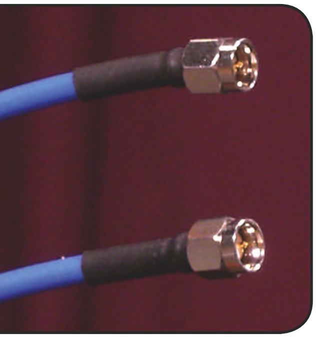
ANALOG DEVICES

BY HOWARD JOHNSON, PhD

Differential coupling

The best-performing, highest-quality, and likely also most expensive differential link you will ever encounter appears on the front panel of an Agilent differential-network analyzer. This spectacularly intricate piece of technology measures differential- and common-mode waveforms going through a test circuit in both forward and reverse directions. It is the gold standard for measurement accuracy when characterizing differential-circuit elements.

An ordinary network analyzer needs only two ports. The two ports make in and out connections to your test circuit. In operation, one port at a time emits a standard test signal while the other measures the received-signal level. The recorded gain, after correcting for all known losses in the measurement apparatus, equals the transmission gain through your test circuit.



The same apparatus also measures the input and output impedance of the test circuit. In that mode, one port at a time emits a standard test signal while measuring the level of signals reflected back from the test-circuit interface. Reflection measurements are quite sensitive to delays and losses in the equipment cables. The cables must be carefully calibrated before making any kind of impedance (S11 or S22) measurements.

A differential-network analyzer works along the same principles, except that each port stimulates the circuit with either a differential- or a common-mode signal. Each port distinguishes the same types of signals at its point of measurement. Those features give the instrument tremendous flexibility in measuring all patterns of differential-to-differential or differential-to-common-mode effects.

If you expect the analyzer to provide data of utmost precision, the cables connecting the analyzer to the device under test must be of the highest quality. Obviously, they must convey differential signals with extreme clarity.

What kind of cables do you think the engineers at Agilent chose for their differential link? If you had to pick a differential-transmission medium that performed well beyond 20 GHz, what would you pick? Would you use a super-tightly coupled differential twisted pair, a quad configuration, or something more exotic?

Think again. Port 1 on the Agilent differential-network analyzer uses two single-ended coaxial cables. It is that simple. Port 1 stimulates the differential mode of transmission at your test circuit using two completely independent, totally uncoupled, not-even-near-each-other coaxial cables. Port 2 uses a second pair of coaxial cables, making four cables in all.

The coaxial cables are precisely symmetric. They are also beautifully shielded and have very low loss. The system performance hinges on their extreme symmetry, not tight coupling. The engineers who built this equipment knew what they were doing. Differential links do not need tight coupling to work effectively.

The same theory applies to your PCB (printed-circuit board). The individual elements of a differential pair need not be pressed close together. They do their job, as long as they are symmetric with respect to the nearest reference plane and are precisely the same length.

If layout density is your greatest concern, then pressing the elements of each differential pair close together may make sense. Pressing them close does save space. To save that space, however, you must first determine how skinny to make the lines to attain the correct differential impedance and deal with the inherent manufacturing uncertainties of making tiny, thin PCB traces.

On the other hand, if density is not a great concern, then leave your traces relatively widely spaced, as you would any ordinary traces on the same board. Control crosstalk by pushing other traces far away. When you change reference planes or go through package or connector boundaries, make sure the traces of each pair are skew-aligned with respect to the receiver.

With these simple rules, your traces may not perform as well as the highly vaunted Agilent differential-port interface, but they will do as well as any other differential traces ever laid on a PCB.**EDN**

Howard Johnson, PhD, of Signal Consulting, frequently conducts technical workshops for digital engineers at Oxford University and other sites worldwide. Visit his Web site at www.sigcon.com or e-mail him at howie03@sigcon.com.

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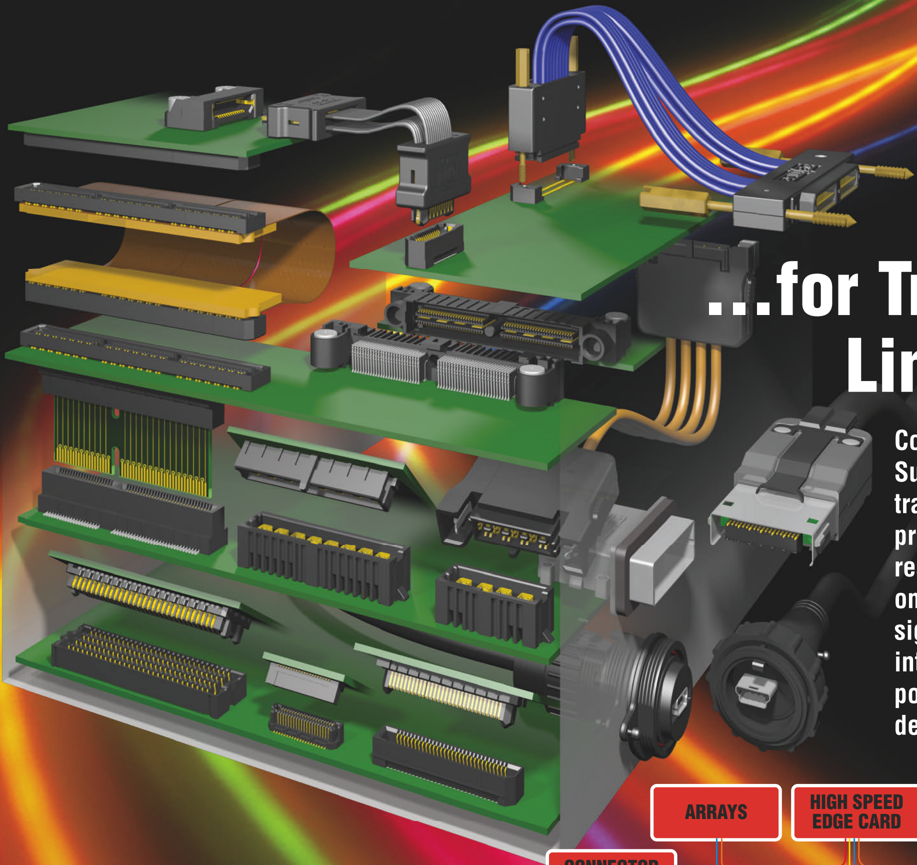


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EDN HANDS-ON PROJECT

SOLID-STATE DRIVES CHALLENGE HARD DISKS

HARD-DISK-DRIVE VENDORS ASSERT THAT MORE-THAN-50-YEAR-OLD ROTATING STORAGE WILL REMAIN RELEVANT FOR MANY YEARS TO COME. SOLID-STATE-DRIVE SUPPLIERS SCOFF AT THESE CLAIMS, CALLING HARD-DISK TECHNOLOGY A HAS-BEEN. WHICH CAMP IS RIGHT?

BY BRIAN DIPERT • SENIOR TECHNICAL EDITOR

Judging from both direct feedback and *EDN*'s Web-site-traffic statistics, engineers have broad interest in the tug of war between currently dominant magnetic hard drives and rapidly rising flash-memory-based solid-state drives. As a result, this hands-on project focuses on that technological battle. The project will live on as a series of online addenda (see **sidebar** "Head to the Web for more hard-drive data"). If cost per gigabyte is your dominant storage metric and especially if you measure your storage needs in triple-digit-gigabyte capacities, hard drives are currently your likely choice. Flash-memory costs are continually plummeting, however. The widespread production ramp-up of cost-effective MLC (multilevel-cell) technology has accelerated flash-memory prices' downward trend.

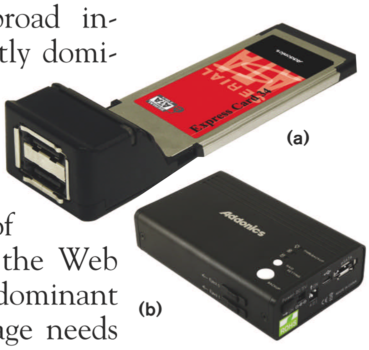


Figure 2 Addonics Technologies' ExpressCard eSATA adapter (a) and portable dual-drive RAID enclosure (b) were among the key pieces of hardware I employed.

Regularly revisiting the comparison of hard-disk drives with solid-state drives makes sense, therefore, particularly considering that the burgeoning per-platter capacities of hard-disk drives may eliminate them from contention if your design's storage demands don't need that much capacity. Solid-state storage also delivers additional potential benefits: It lacks a motor to drive one platter or multiple platters spinning at thousands of rotations per minute. It also lacks a vacillating read/write head—or several heads—hovering only a few millionths of an inch above the magnetic material. The lack of these attributes gives solid-state drives better shock tolerance; long-term reliability; and, depending on your usage scenario, power consumption than hard-disk drives.

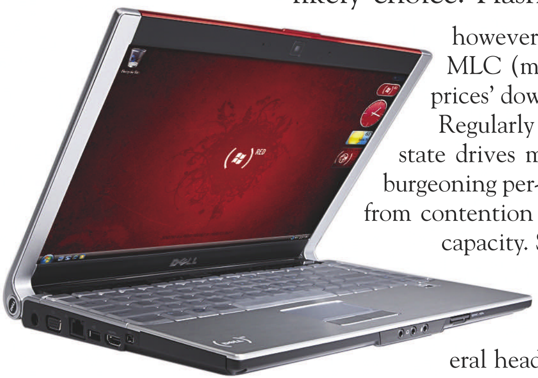


Figure 1 Dell's XPS M1330 proved to be a capable test bed for my hard-drive and solid-state-drive project.

Solid-state drives are also immune to magnetic-field-cultivated data-corruption effects, and they operate silently. Plus, the lack of rotating-media-incurred delays can deliver tangibly shorter seek times for solid-state drives than for hard-disk drives. This performance is especially noticeable with systems requiring a lot of random-access tasks, and it is particularly so when most of those accesses are reads rather than writes. Access performance is the focus of this article.

I had originally planned to use the same Apple MacBook I employed for an earlier article (**Reference 1**). Doing so was conceptually appealing due to the fact that the device lets you boot OS X not only from an optical disc or internal hard drive but also from a FireWire-tethered or, with newer Intel CPU-based systems, USB-tethered external hard-disk drive. I therefore obtained a generic SATA (serial-advanced-technology-attachment)-extender cable that mates with the system's internal-drive connector and enables hot-swap of drives under test. I also got a 2.5-in. IEEE 1394 SATA enclosure from Addonics Technologies for my system's main drive. Although I own plenty of USB 2 enclosures, a FireWire alternative was appealing both because the data-interface cable would also supply sufficient current to power the hard-disk drive and because of the interface's likely faster performance than USB 2 (**Reference 2**).

Upon further analysis, however, my first-pass strategy began to dissolve. To use the SATA-extender cable, I would have had to remove the system battery and therefore run the system solely off ac power. Unfortunately, MacBooks automatically throttle the system clock down to 1 GHz when no battery is present (**Reference 3**). This quirk wasn't a deal breaker; between drive tests, I'd alternatively just need to power down the system, remove the battery, swap drives, replace the battery, and boot up again. I then discovered, however, that the

AT A GLANCE

- Careful system-component selection is essential to ensuring that storage subsystems succeed or fail without unfair hindrance by bottlenecks out of their control.
- The rotations-per-minute figure is only one of several fundamental parameters that define hard-disk-drive performance; also consider areal-storage density, cache-buffer size, and other specifications.
- MLC (multilevel-cell)-flash-memory-based solid-state drives trade off lower read and write performance, at least in theory, for lower cost per gigabyte than their SLC (single-level-cell)-based solid-state-drive counterparts.

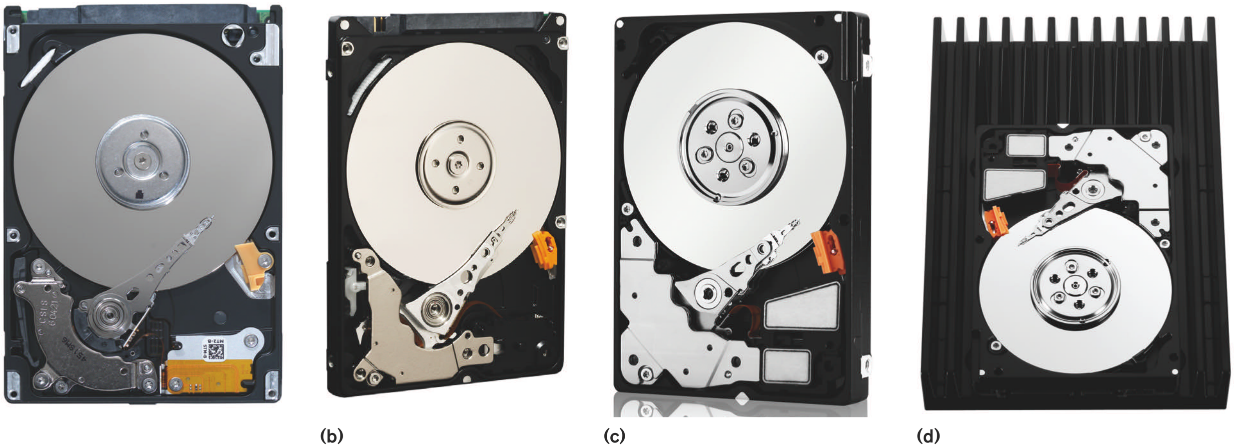


Figure 3 I tested Seagate's 7200-rpm hard-disk drive (a) and Western Digital's 5400-rpm drive (b) and 2.5- and 3.5-in., 10,000-rpm units (c and d).

HEAD TO THE WEB FOR MORE HARD-DRIVE DATA

When Intel introduced its SLC (single-level-cell) and MLC (multilevel-cell)-flash-memory-based solid-state drives at mid-August's Developer Forum, officials indicated that the company would within 90 days be shipping SLC-derived units. In mid-October, though, the company announced that SLC solid-state drives were ready for sale, one month earlier than previously indicated. As a result, I hope to have my hands on a review unit—or, preferably, two units, for RAID 0 testing—by mid-November. I'll pass along benchmark results on the *Brian's Brain* blog on *EDN*'s Web site at www.edn.com/briansbrain. I'm especially curious to see whether these drives outperform their already-tested MLC relatives in write performance. Micron has also been since mid-July promising solid-state drives for review, but shipping schedules have steadily slipped. If the company's vows ever translate into hardware in hand, I'll also use the blog to transfer these drives' stats to you. For the drives that I've tested for this project, I'll provide downloadable links for the raw Sandra ASCII-text-report files, along with an Excel-spreadsheet consolidation of their data.

I also plan for the online augmentation of this article to include a description of the Sandra tests I ran for this project so that you can understand what holes might exist in my research. You might want to plug these holes or address concerns about your unique design criteria with findings from your own projects. I'll include not only relevant sections of Sandra's user guide but also more in-depth explanations that SiSoftware's Adrian Silasi, lead programmer for the company's Sandra program, crafted at my request. Finally, I'll explain why—aside from practical manpower and time constraints—I didn't pursue additional benchmarking, such as system boot time, application-specific launch time, power consumption, and battery-life comparisons.

core-logic chip set in my MacBook supports only SATA's first-generation 1.5-Gbps speeds. Almost all of the drives I would be testing were SATA/300—that is, 3 Gbps, and I didn't want the chip set to act as an artificial constraint on their full performance potential.

Instead, I went with my Windows Vista-based Dell XPS M1330 laptop, whose Santa Rosa ICH8M chip set complies with SATA/300 (**Figure 1** and **Table 1**). I then faced another quandary, however: You can't boot Windows Vista from an external hard drive. Instead, I could have cloned a common NTFS (New Technology File System) image to each hard-disk and solid-state drive I was testing, sequentially installing each in the system's internal drive bay. Whenever I booted the XPS M1330, however, I'd need to revalidate the operating system with a new registration key because the detected hardware change would prompt a Windows-product-activation alert.

Instead, I dodged the hassle by using Addonics' ExpressCard eSATA (external-SATA) adapter to test the hard-disk and solid-state drives (**Figure 2**). Because ExpressCard's 2.5-Gbps speed places a limitation on SATA's 3-Gbps performance, I couldn't run the drives at their highest possible transfer rates. My mass-storage-benchmark program of choice, as has been the case in many past projects, is SiSoftware's Sandra. This time around, I used the company's free latest version, the 2000 Lite edition.

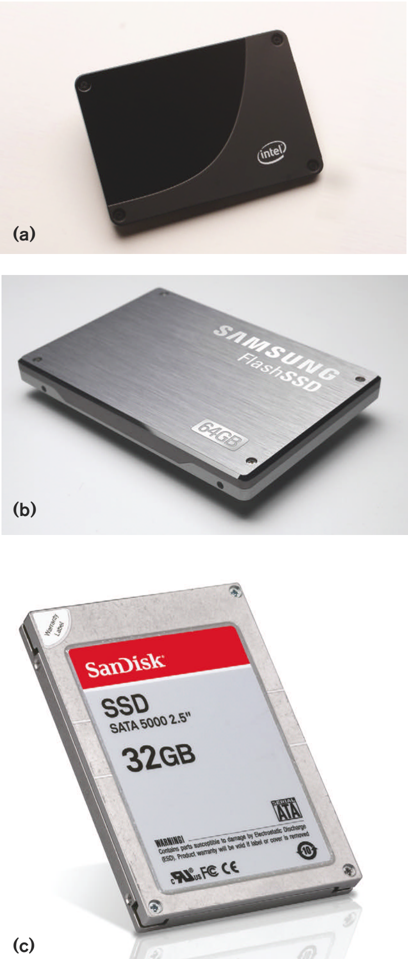


Figure 4 I used two of Intel's multilevel-cell flash-memory-based solid-state drives (a), which enabled me to do some interesting RAID 0 testing. I also tested a single-level-cell solid-state drive from Samsung (b) and an older design from Sandisk (c).

In addition to the hardware that Addonics provided, Bill Kwong, the company's president, also donated an eSATA-to-SATA adapter cable; a stand-alone SATA power supply; and, because I had the good fortune to get my hands on two Intel solid-state drives, a dual-slot eSATA enclosure capable of RAID (redundant-array-of-inexpensive-disks) 0, JBOD (just-a-bunch-of-disks), RAID 1, and other multidrive-mode operation. As you'll soon see, the dual-slot enclosure yielded unexpected results.

Figure 3 and **Table 2** depict the hard-disk drives I evaluated for this project. Note that all the hard drives are recent-generation units. This selection was intentional because it ensured that all of the drives employed high-capacity PMR (perpendicular-magnetic-recording) technology. An earlier longitudinal-recording-based drive would have had a lower bits-per-square-inch areal density and would consequently incur a substantially lower transfer rate than PMR at given rotations-per-minute figures. Successive PMR-technology iterations have been delivering incremental storage capacities, however, so the rotations-per-minute-normalized bit-packing metrics of the drives I tested aren't necessarily equivalent. For example, Seagate sent me a Momentus 7200.2 drive instead of a newer and denser 7200.3 unit.

Unfortunately, I couldn't obtain a 4200-rpm hard-disk drive; such drives find use in ultralow-cost and ultralow-power—albeit ultralow-performance—applications as well as in systems that strive to squeeze the maximum storage from a platter. Such drives are largely falling out of favor, however, as 5400-rpm variants become more power-efficient, dense, and cost-effective over time. My single-platter, 5400- and 7200-rpm drives came from Western Digital and Seagate, respectively, and Western Digital also supplied me with high-end, 10,000-rpm units. On a hunch, I tested both the company's 2.5- and 3.5-in. VelociRaptor drives; the 3.5-in. device comprises an IcePack heat sink surrounding a 2.5-in. drive. According to the company, the two drives should deliver identical results, but they didn't, perhaps because of differences in their firmware.

To understand why I included three solid-state drives in this project, you need to first understand some high-level differences between SLC (single-level cell)- and MLC-flash technology (**Figure 4** and **Table 3**). Intel's drive employs MLC techniques. It stores 2 bits of information within each flash-memory-array transistor by equating a unique 2-bit data combination with each of four possible charge amounts

TABLE 1 SYSTEM SPECIFICATIONS

Model	Dell XPS M1330
Operating system	Microsoft Windows Vista Ultimate SP1, 32-bit
CPU	Intel Core 2 Duo T5450: 65-nm, 1.66-GHz-core-clock, 667-MHz-front-side-bus Merom with a 2-Mbyte L2 cache
Core-logic chip set	Intel Santa Rosa Mobile 965 Express with GMA X3100 integrated graphics and ICH8M south bridge
Memory	4-Gbyte Kingston DDR2-667 comprising two 2-Gbyte SoDIMMs
Integrated hard-disk drive	Seagate ST9160821AS (Momentus 5400.3, SATA/150 interface, 5400-rpm, 8-Mbyte cache buffer)

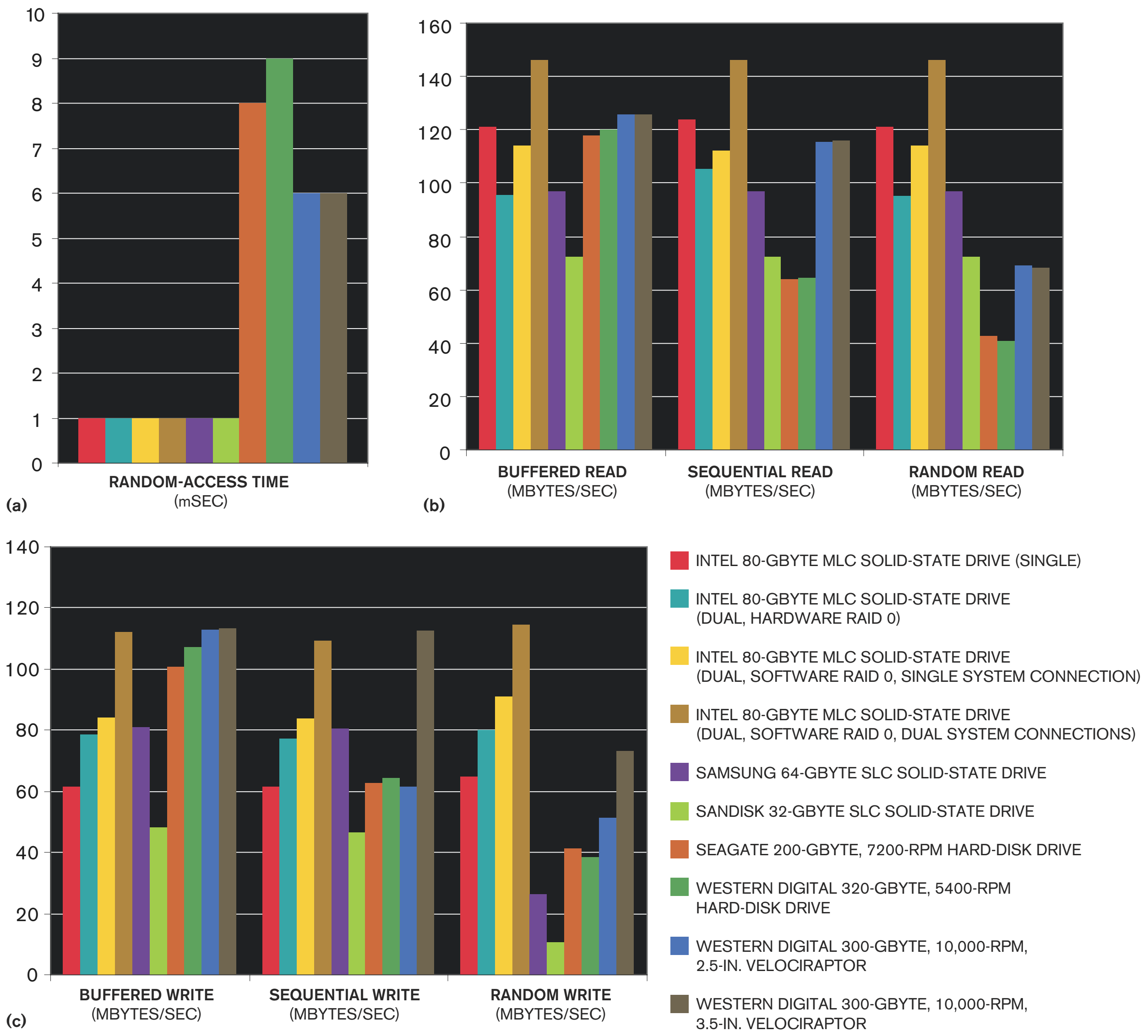


Figure 5 Sandra's File Systems results provided a solid foundation for subsequent analysis: random-access time (a), various read tests (b), and an assortment of write experiments (c).

on the transistor's floating-gate structure. This arrangement translates to three threshold levels that act as the boundary conditions. Sensing the exact charge value during read operations takes more time than does the traditional SLC approach, which differentiates between only two charge-quantity states—that is, a single threshold level. However, MLC extracts 2 bits' worth of information at a time—versus 1 bit per transistor access for SLC—counterbalancing the extended MLC-read-access delay.

MLC performance suffers even more during write operations, however. Depositing a precise number of charge electrons on the floating gate is critical

TABLE 2 HARD-DISK-DRIVE SPECIFICATIONS

Supplier	**Product**	**Capacity** (Gbytes)	**Interface**	**Cache-buffer size** (Mbytes)	**Speed** (rpm)
Seagate	ST9200420ASG Momentus 7200.2	200	SATA/300 with native-command queuing	8	7200
Western Digital	WD3200BEVT Scorpio Blue	320	SATA/300 with native-command queuing	8	5400
Western Digital	WD3000BLFS (2.5-in. VelociRaptor Version 4.0)	300	SATA/300 with native-command queuing	16	10,000
Western Digital	WD3000GLFS (3.5-in. VelociRaptor Version 3.0)	300	SATA/300 with native-command queuing	16	10,000

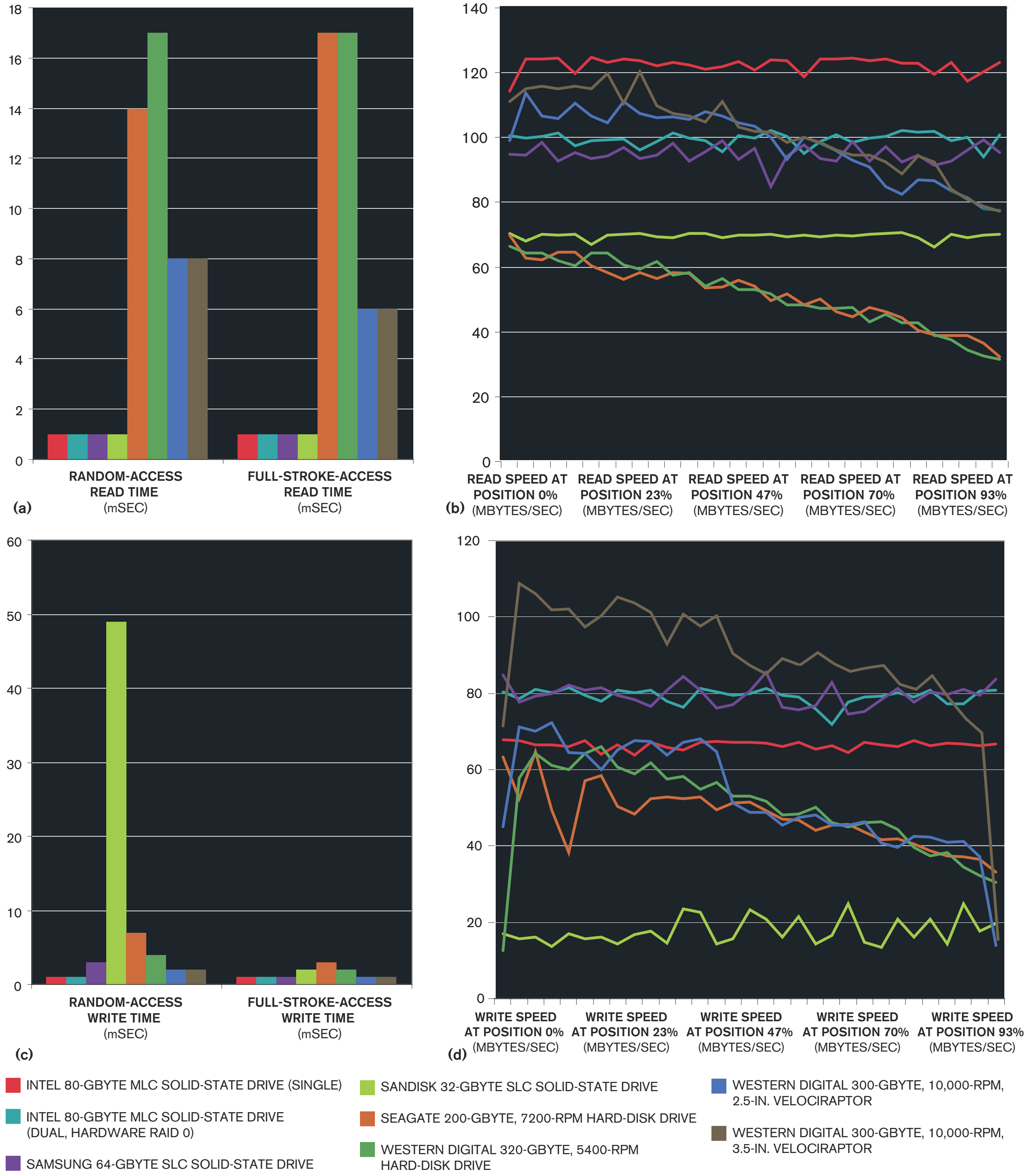
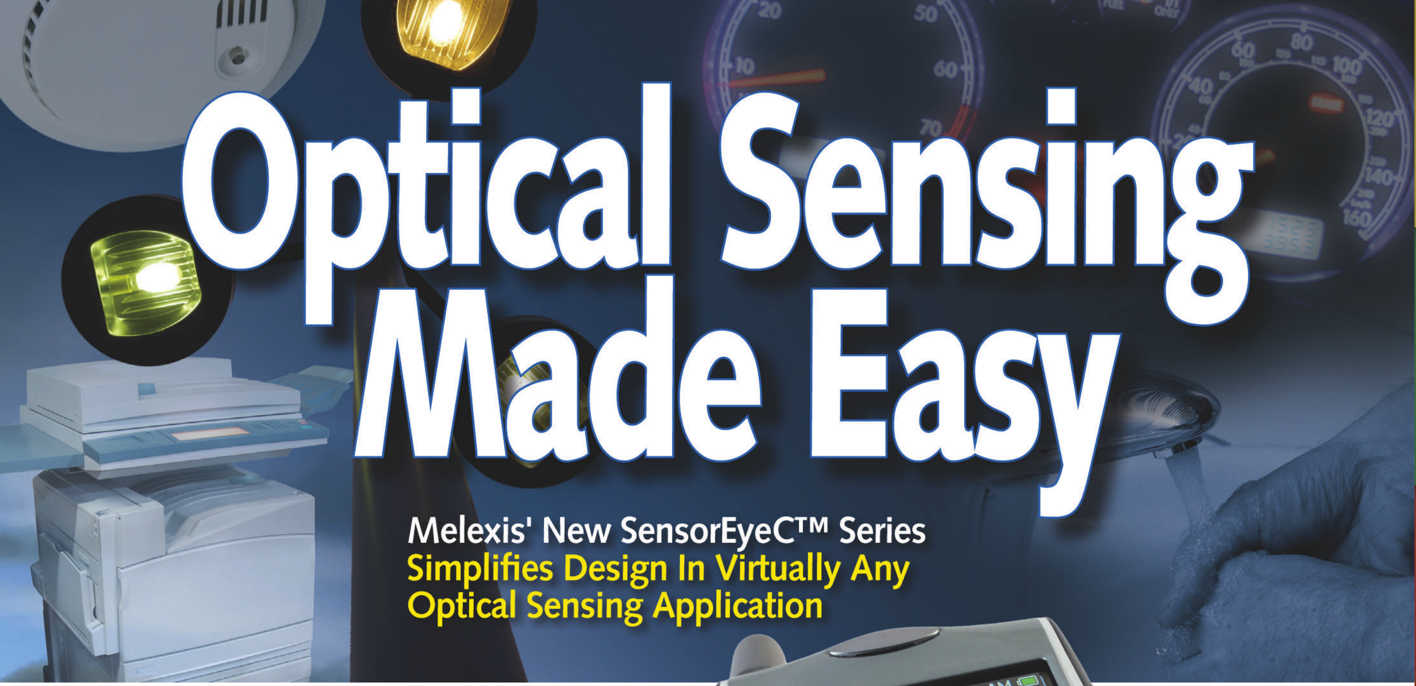


Figure 6 Eliminating the operating-system intermediary with the Physical Disks benchmarks resulted in additional useful data: average and percentage-of-total-capacity-dependent read-access times (a and b, respectively) and average and percentage-of-total-capacity-dependent write-access times (c and d, respectively).

TABLE 3 SOLID-STATE-DRIVE SPECIFICATIONS

Supplier	Product	Capacity (Gbytes)	Interface	Cache-buffer size
Intel	SSDSA2MH080G15E	80 (multilevel cell)	SATA/300 with native-command queuing	Not reported
Samsung	MCCOE64G5MPP-0VA	64 (single-level cell)	SATA/300 with native-command queuing	64 Mbytes
Sandisk	SDS5C-032G-000000	32 (single-level cell)	SATA/150	0



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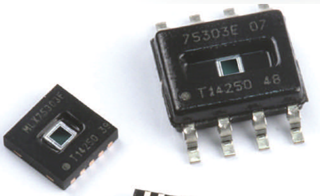

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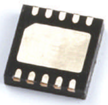

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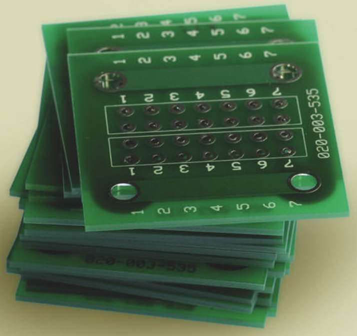


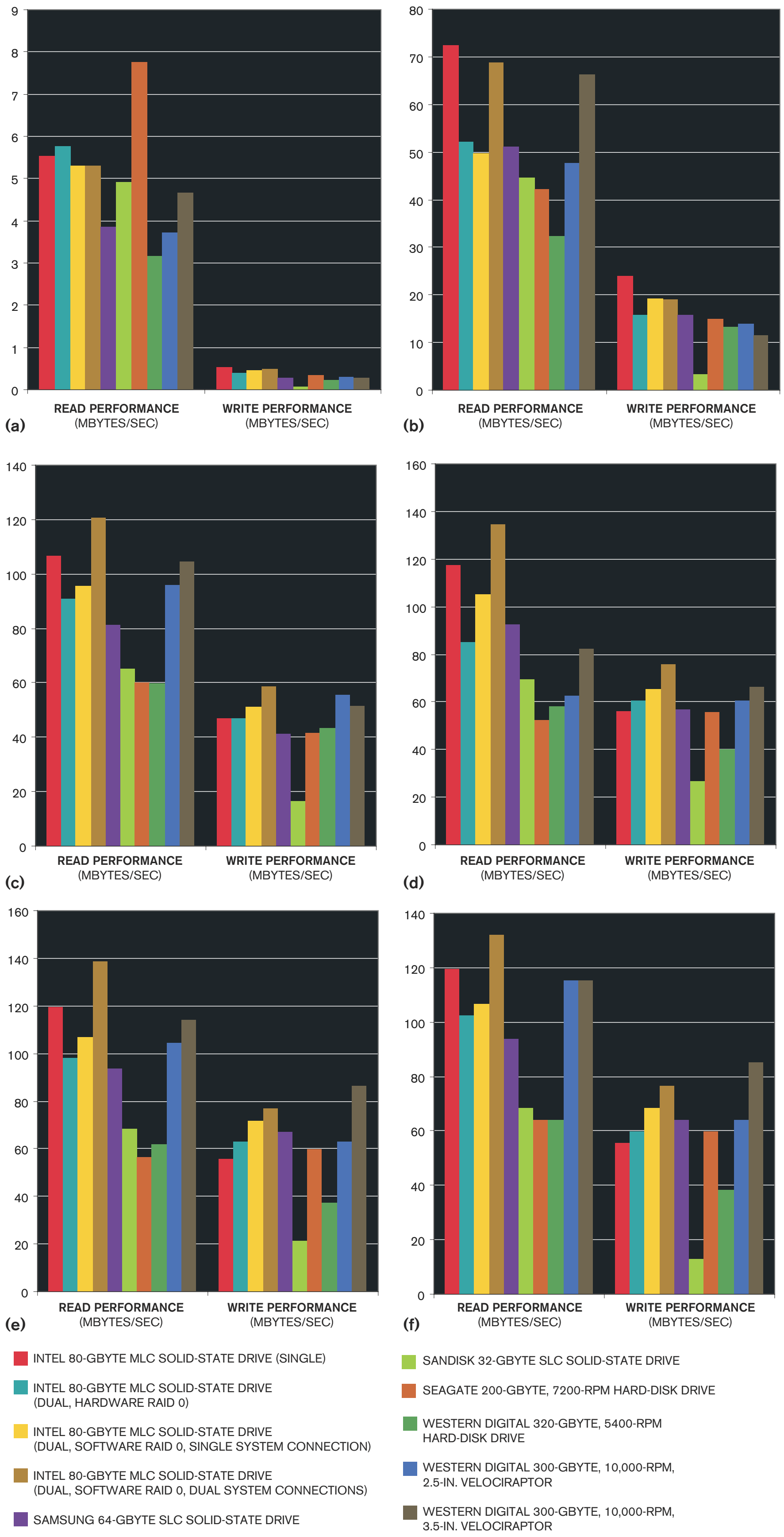
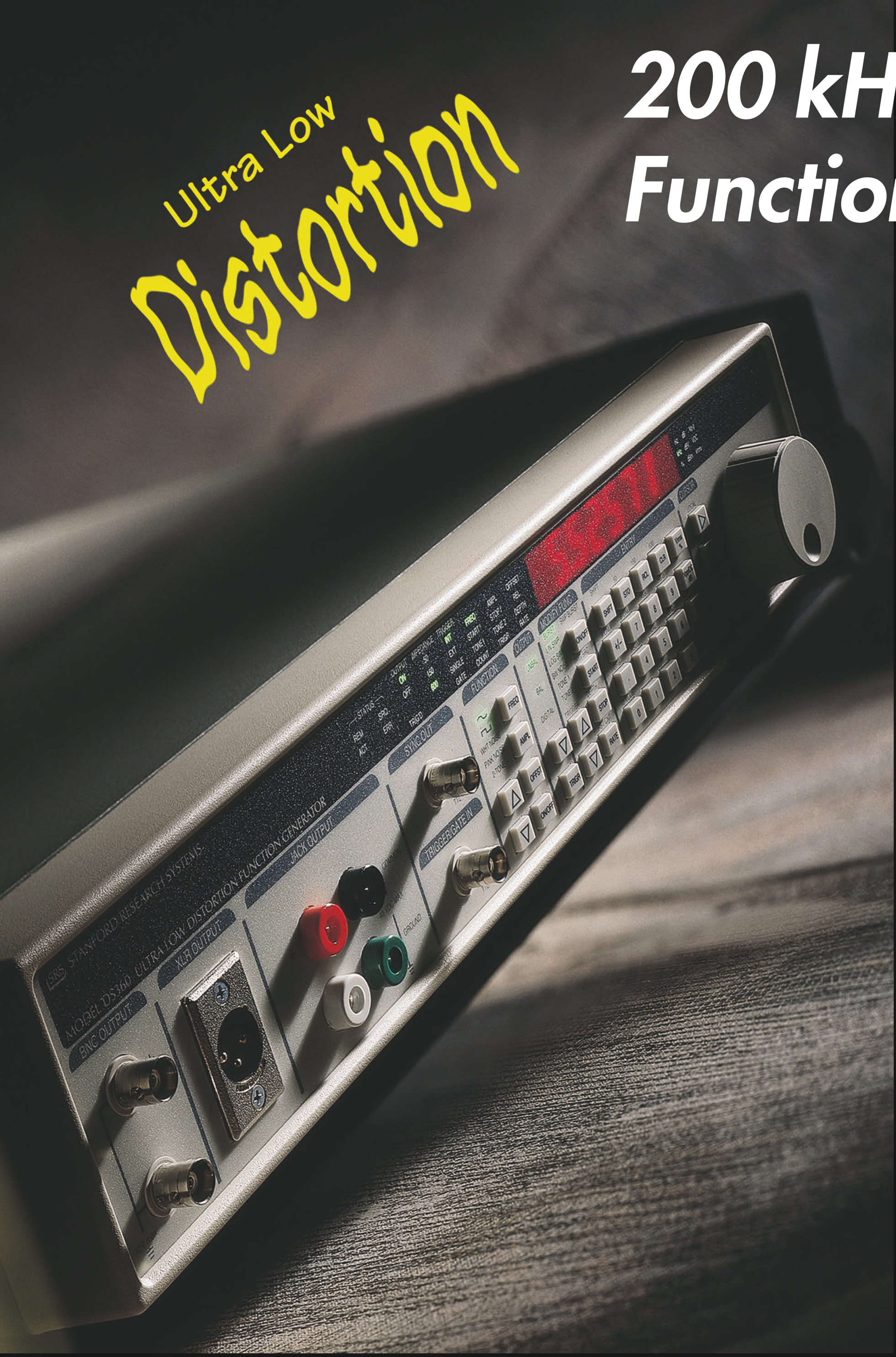


Figure 7 Sandra's Removable Storage test quantified drive performance as a function of file payload size: 512 bytes (a), 32 kbytes (b), 256 kbytes (c), 2 Mbytes (d), 64 Mbytes (e), and 256 Mbytes (f).



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to ensuring accurate subsequent readback results, particularly when you consider that the ensuing data alteration of adjoining transistors can result in minor charge disturbances of the transistor in question. SLC-write operations, conversely, can be more brute force in nature and consequently faster. Therefore, I tested one SLC-based solid-state drive from Samsung, another from Sandisk, and an MLC-based drive from Intel. Sandisk's drive is nearly two years older than Samsung's; embryonic solid-state-drive technology is on a rapid improvement ramp, according to the suppliers. I wanted to see whether that claim translated to noticeable benchmark differences between the two SLC-solid-state-drive contenders.

FLASHY FILE-SYSTEM RESULTS

Sandra's File Systems test encompasses the Windows Vista SP1 intermediary, meaning that it operates at the INT 21 level, not the INT 13 BIOS level (**Figure 5**). The results show that Sandra rounds up all access-time measurements to the nearest millisecond, thereby explaining why all of the solid-state drives reported 1-msec random-access times. Future Sandra versions will deliver microsecond-level precision, however, according to Adrian Silasi, lead programmer for the Sandra team at SiSoftware. Nonetheless, solid-state-storage subsystems' random-access ability gives them a clear advantage over rotating-media alternatives. Solid-state drives' read-performance advantages over hard-disk drives predictably become more apparent with more random-access patterns. A close parity also exists between Western Digital's 5400-rpm drive and Seagate's 7200-rpm alternative, perhaps reflecting the fact that the newer Western Digital drive employs a more aggressive PMR-areal-density specification.

The older Sandisk SLC-flash-memory-based solid-state drive also lags behind both the Intel MLC- and Samsung SLC-flash-memory-based solid-state drives in both read and write tasks. I suspect that the Sandisk unit's lack of an onboard RAM buffer is partly to blame. In contrast, Samsung's solid-state drive reportedly embeds a massive 64-Mbyte buffer. Intel declined to reveal a cache-buffer size for the company's solid-state drives. Other reasons for the Sandisk drive's inferior showing may be the fact that it uses an earlier-generation, lower-performance NAND-flash-memory foundation, and the fact that it simultaneously accesses fewer flash-memory components.

⊞ See the "Solid-state-drives-challenge-hard-disk drives" posts at www.edn.com/briansbrain for supplemental information on this article's topics.

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Another surprise occurred when I compared the single-drive-read performance of Intel's solid-state drive with the dual-drive-RAID 0-striped performance in Addonics' enclosure: Addonics' dual-drive configuration operates at a lower speed than a single Intel device. The Addonics portable dual-drive-RAID enclosure embeds a Silicon Image SteelVine SATA RAID processor. Based on the numbers, I suspect that this processor was acting as a performance bottleneck to the solid-state drives behind it. I therefore added two other hardware configurations to my test suite. The first continued to employ only the Addonics enclosure; instead of configuring the drives in hardware-RAID 0 mode, however, it used a JBOD configuration. Windows Vista's built-in software running on an Intel CPU alternatively performed RAID 0 striping, increasing performance. For my final test, I left one Intel solid-state drive in the Addonics enclosure but tethered the other one directly to the second eSATA port in the ExpressCard adapter. Again, moving the performance bottleneck closer to the Dell laptop resulted in a performance boost.

Solid-state-drive results differed somewhat in the write tests, although the overall hardware-versus-software RAID trends held steady. Dual-drive writes completed faster than single-drive counterparts, even when I controlled them with hardware within the Addonics enclosure. This result reflects the fact that dual-drive RAID 0 parallel-write striping inherently counterbalances slow MLC-flash-memory writes. Don't conclude from these statistics that hardware RAID is inherently bad. I ran my tests with a lightly used system CPU; the software-RAID results may have been substantially worse in a more heavily loaded situation, whereas the hardware-RAID outcomes would have been largely independent of CPU loading. As I expected, too, Samsung's SLC-flash-memory solid-state drive outperformed Intel's MLC-based alternative on single-drive-write tests.

PHYSICAL-DISK DEDUCTIONS

After removing the operating-system intermediary, I tested to see how these drives would respond to Sandra's Physical Disks direct-access analyses, which provide not only average access times for the entire drive but also statistics for various capacity thresholds across the drive (**Figure 6**). In examining the data, remember that the drives I tested for this project had various capacities. One of the first things you'll probably notice is that the hard-disk drives all exhibit classic access-performance degradation as the read/write heads move across the platters, whereas solid-state-drive-access speeds are consistent across the capacity range.

Again, you'll see worse performance for a hardware-RAID 0 read for the two-drive-striped Intel solid-state configuration using Addonics' enclosure than that of the single-drive alternative. Unfortunately, in this case, I couldn't test the software-RAID-substitute approach because it would have required that I partition the setup with an NTFS format, which is incompatible with Sandra's Physical Disks test requirements. Note, too, the degraded write performance for several of the hard-disk drives at both extremes of their capacity ranges. Also, although the 2.5- and 3.5-in., 10,000-rpm Western Digital drives are supposedly identical at their cores and consequently had comparable read-access attributes, the 3.5-in. drive, which comes with a heat sink, delivered considerably higher write performance than its 2.5-in. sibling.

To gain an even greater understanding of the drives' capabilities, I turned to Sandra's Removable Storage tests, which subjected the storage subsystems to read and write sequences comprising six file sizes (**Figure 7**). As you peruse the results, you'll likely notice that the drives' designers optimized firmware and other factors for certain file sizes—to the detriment of others. Again, look at the write performance of the two supposedly identical, 10,000-rpm Western Digital drives: Whereas the 2.5-in. drive held the lead with small payloads, its 3.5-in. counterpart surpassed it once file sizes exceeded the 1-Mbyte threshold. And, because I was working with NTFS-formatted drives, I was able to test all three RAID 0 configurations with the two Intel solid-state drives.EDN

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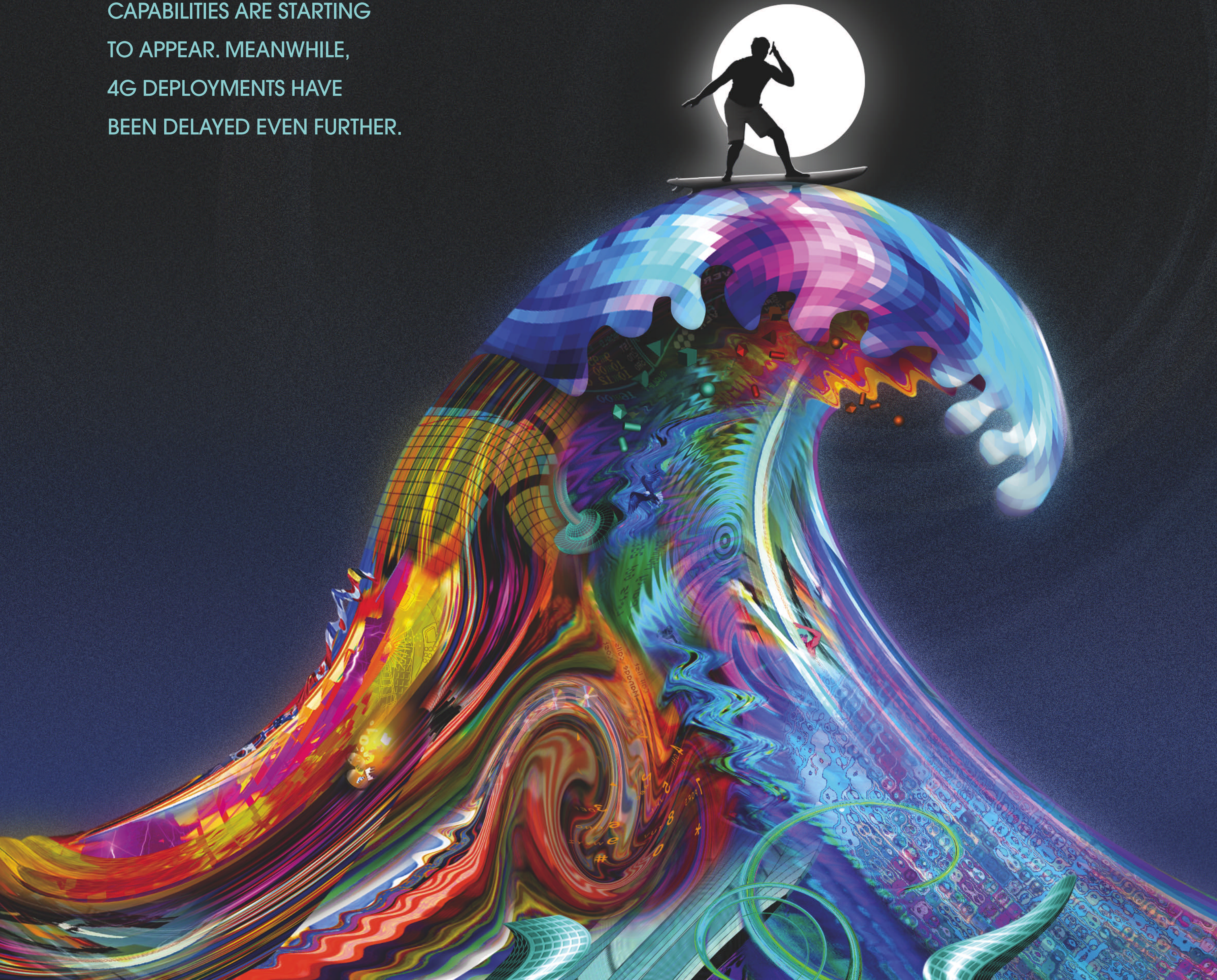
3G WIRELESS DATA: about to break?

ALTHOUGH THE DEFINITIONS OF 3 AND 4G WIRELESS DATA NETWORKS, SERVICES, AND TERMINALS HAVE BEEN MOVING TARGETS, SOME LONG-PROMISED 3G CAPABILITIES ARE STARTING TO APPEAR. MEANWHILE, 4G DEPLOYMENTS HAVE BEEN DELAYED EVEN FURTHER.

BY ANN R THRYFT • CONTRIBUTING TECHNICAL EDITOR



The rollout of 3G (third-generation) wireless data networks began in Japan as early as 2001, but the first 3G network didn't appear in the United States until 2002. Major rollouts began here a few years later. With the release of Apple's iPhone 3G in July, consumer expectations about media availability and access began running high. The appearance of competitive 3G phones, such as Google's open-standard, no-license-fee, OS-based Android platform, will likely drive those expectations even higher (see **sidebar** "3G handsets"). But is the entire network infrastructure ready for simultaneous data download and upload traffic by even half of the world's 3 billion cell-phone users if they all decide to attempt social networking, mobile-video transactions, or both at the same time? Even though new 4G (fourth-generation) standards are in the offing for improving latency and other problems in cell-access networks, what about the backhaul networks, head ends, and network cores?

Whether 3G networks are well under way or just beginning depends on your geographic location, how you define the set of features, and which part you are considering: network infrastructure, data services, or handsets. The definitions of 3 and 4G-network technologies and services and the boundaries between generations have shifted over the last few years (see **sidebar** "3 and 4G definitions and technologies" in the Web version of this article at www.edn.com/081113cs). To some extent, this situation is happening because 3G-network buildouts, handset development, and data services did not become available together in lock step. Originally, 3G meant data services—not just texting, e-mail, and IM (instant messaging), but also full-fledged Web browsing and data downloads and uploads over high-speed Internet-broadband links, as well as video-telephone calls. Yet, current 3G networks and services have been unable to deliver sustained data rates high enough to support video of 10 Mbps or more.

Meanwhile, even more air-interface standards have proliferated, especially if you count shorter-range wireless protocols, such as Wi-Fi and Bluetooth. A not-uncommon view of what 4G mobile devices will accomplish is the ability to handle several air interfaces from multiple base stations and negotiate with them more or less simultaneously while processing multiple types of data and services switching in real time. This ability was one early vision of 3G.

The ITU (International Telecommunications Union) has defined 3G wireless communications under the IMT-2000 standard and named five qualifying air interfaces: W-CDMA (wideband-code-division multiple access), CDMA2000, TD-CDMA/TD-SCDMA (time-division CDMA/time-division-synchronous CDMA), EDGE (enhanced-data-rates-for-global evolution), and DECT (digital-enhanced-cordless telecommunications). Last year, the ITU added mobile WiMax (worldwide interoperability for microwave access) as a sixth. Nearly every major operator has 3G today, says Allen Nogee, In-Stat's principal analyst for wireless technology and infrastructure.

Yet, according to a new In-Stat study, says senior analyst Gemma Tedesco, through 2012, most cell subscriptions will be for GSM (global-system-for-mobile) communications, a 2G technology, and the 2.5G GPRS (general-packet-radio service) (**Figure 1** and **Reference 1**). "Even CDMA2000 is being used only for texting and voice, not for data," she says. HSPA (high-speed packet access) has grown in Western Europe, but, even in 2013, there will still be huge amounts of GPRS and EDGE. Most operators in the world haven't built out 3G networks. Where they have, such as in Asia and most of South America, not all cell users have 3G-capable devices. In the United States, most operators have 3G networks, and lots of users have 3G devices without paying for 3G data service. "So, 3G is not really here yet around the world," she says.

Meanwhile, according to recent In-Stat research, although carriers rolled out many new

3G networks worldwide in 2007, overall shipments of cell base stations in 2008 declined considerably (**Reference 2**). “New 3G networks are continuing to be deployed,” says In-Stat's Nogee in a press release. “However, the worldwide economy has been faltering, subscriber-GSM growth—even in fast-growing developing areas—is starting to slow, and wireless broadband use, while growing, is not growing fast enough for operators to spawn continued base-station growth.”

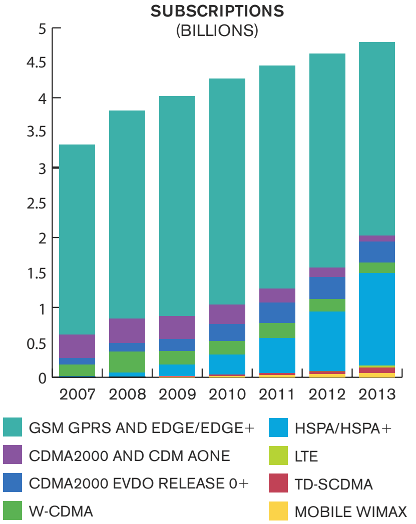


Figure 1 Through 2012, most cell subscriptions will be for GSM, a 2G technology, and the 2.5G GPRS (courtesy In-Stat).

Many industry observers talk about nimbleness and flexibility, so that cell phones and other access devices, such as notebook PCs, will make the most effective connection possible, given the application, the location, and the available services and networks. The picture that emerges is a patchwork of multiple broadband-wireless-access technologies and services. To some extent, this image also applies to the backhaul.

WHAT ABOUT THE BACKHAUL?

Published discussions of the increased data traffic expected in 3 and 4G networks rarely mention the effect on backhaul networks and the network core. Yet, equipment and technology in this area are at least as vital to the network as access and terminal-device technologies. Carriers have a variety of choices to consider, as well as a number of issues to manage for increased data traffic, especially as that traffic begins to move onto higher-frequency 4G networks.

AT A GLANCE

- Most US operators now have 3G (third-generation) networks, but few subscribers have 3G service.
- The definitions of 3 and 4G (fourth-generation) network technologies and services and the boundaries between generations have shifted over the years.
- Even more air-interface standards have proliferated, and 4G mobile devices will need to handle multiple air interfaces from multiple base stations.
- The first major 802.16e mobile-wireless WiMax (worldwide-interoperability-for-microwave-access) network in the United States debuted in September, when Sprint rolled out its Xohm network for carrying voice, video, and data.

As demands on the backhaul and net-

3G HANDSETS

In handsets, 3G (third-generation) technology is gaining momentum. The first Google Android-based 3G phone, the G1 from 3G operator T-Mobile, was scheduled to become available last month. In addition to 3G capabilities, it includes an iPhone-like touchscreen and a small keyboard and provides support for GPS (global-positioning-system) navigation and Wi-Fi-Internet access. The Google-led OHA (Open Handset Alliance) developed the Android open-standard, no-license-fee, Linux-based platform.

“Even with 3G, there's been a gap between what handset hardware has been capable of and what software has exposed to the end user as possibilities, such as streaming media,” says Eric Thomas, strategic-marketing manager for open-source software for Texas Instruments' wireless-terminals-business unit. “The [OHA's] software-centric focus will increase the use of services to the levels that users have expected for years, which will, in turn, affect the infrastructure.” Open operating systems from Symbian and Microsoft, and now the Android, may require more memory and processing power than do proprietary operating systems, with their tightly coupled operating systems and silicon, but open systems will also make it easier for developers to write applications, says Ton Van Kampen, vice president of business development for ST-NXP Wireless.

Nokia's answer to the iPhone, with a similar touchscreen and form factor, also debuted last month. The 5800 XpressMusic will become available during the fourth quarter of this year. Based on the Symbian operating system, it includes GPS navigation. The RIM (Research In Motion) touchscreen-only Blackberry Storm, which RIM announced in October, will become available before the end of the year and comes with GPS navigation as well as photo-sharing and Facebook applications. Phones that support 3G networks include the Nokia N95, the RIM Blackberry Bold, and the Verizon LG Dare.

A few phones, including some Blackberry models, can operate on both GSM (global-system-for-mobile)-communications and CDMA (code-division-multiple-access) networks, says Allen Nogee, In-Stat's principal analyst for wireless technology and infrastructure. “But they have to use a separate set of chips, so this kind of dual-mode phone hasn't really taken off. Silicon for 3G phones still draws a fair bit of power, and WiMax [worldwide interoperability for microwave access] will draw even more.” Phones that cost less than $20 are important to still-growing 3G markets, such as India, leaving little in the bill of materials for chip costs. ST-NXP's Van Kampen says that his company is integrating multiple air-interface standards into silicon, including GSM/UMTS (universal-mobile-telecommunications system) and EDGE (enhanced data rates for global evolution).

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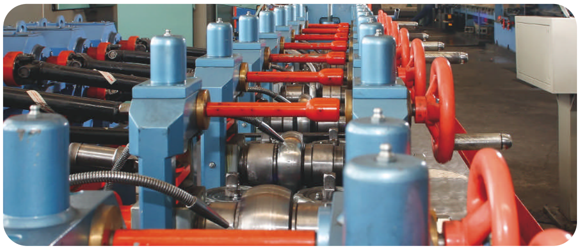
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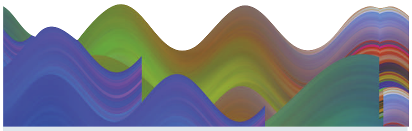
work core increase because of more data-centric services, carriers are shifting from a leased-line model with T1/E1 lines to deploying optical or fiber technology right up to the base station to carry extra capacity, says Jagdish Rebello, iSuppli's director and principal analyst of wireless communications. Instead of taking this traffic back to the base-station controller or switching station, equipment manufacturers are putting more intelligence into the base station. This approach will reduce traffic in the core and reduce latency, especially important for social networking, gaming, and push-to-talk applications. According to Greg Waters, executive vice president and general manager for front-end products for Skyworks Solutions, many operators are focusing on next-generation cell-base-station technology, such as femtocells, that goes beyond 3G (**Figure 2**).

Fulcrum Microsystems' OEM customers require low latency for voice traffic, synchronous Ethernet, and mechanisms for congestion management of voice, video, and data—that is, QOS (quality of service), says Gary Lee, director of product marketing. Voice traffic requires maximum-latency guarantees, and video needs minimum-bandwidth guarantees and somewhat-lower latency, making it difficult to combine them on the same network. Solving QOS issues by throwing extra bandwidth at the problem may have worked in the early cell-network days, he explains, "but now we have thousands of video streams, so QOS mechanisms must be built-in." In silicon, this situation calls for network processors, multicore CPUs, and switch fabrics that can provide minimum-bandwidth guarantees and congestion-management features.

"There's been a significant increase in data utilization in mobile networks, but they aren't necessarily designed to handle QOS," says Todd Mersch, Continuous Computing's senior product-line manager. The problems iPhone 3G users experienced when millions of them first attempted to access AT&T's wireless network exemplify this issue. Deep packet inspection, deployed on wireline networks to prioritize certain types of traffic for QOS, is also seeing more use on mobile networks.

ONE BACKHAUL ALTERNATIVE MAY BE WI-FI IN THE 5.8-MHz BAND AS A SEPARATE RADIO STRUCTURED MESH NETWORK.



If carriers are to leverage cost-effective IP (Internet Protocol) networks to handle the increased bandwidth expected from 3 and 4G services without undue packet loss and call dropping during handoff to the base station, the most critical issue is time synchronization, says Sameer Vuyuyu, vice president of marketing for Semtech's advanced-communications division. One mobile-wireless-network-synchronization scheme, FDD (frequency-division duplex), uses the same technology as wired networks. The other, TDD (time-division duplex), requires finely tuned frequency accuracy and phase alignments among all base stations in the cell network. The current GPS-synchronization system, comprising a master GPS clock and hundreds of GPS slaves, works inconsistently inside buildings and can be expensive to implement. Competing methods that transmit clock data over packet-switched networks include the IEEE 1588 Version 2 Precision Time Protocol standard for network-based timing and synchronization, which the IEEE finalized last March. "The master still needs a GPS module, but now you're amortizing that cost over hundreds of less-expensive slaves," says Vuyuyu.

One backhaul alternative may be the use of Wi-Fi in the 5.8-MHz band as a

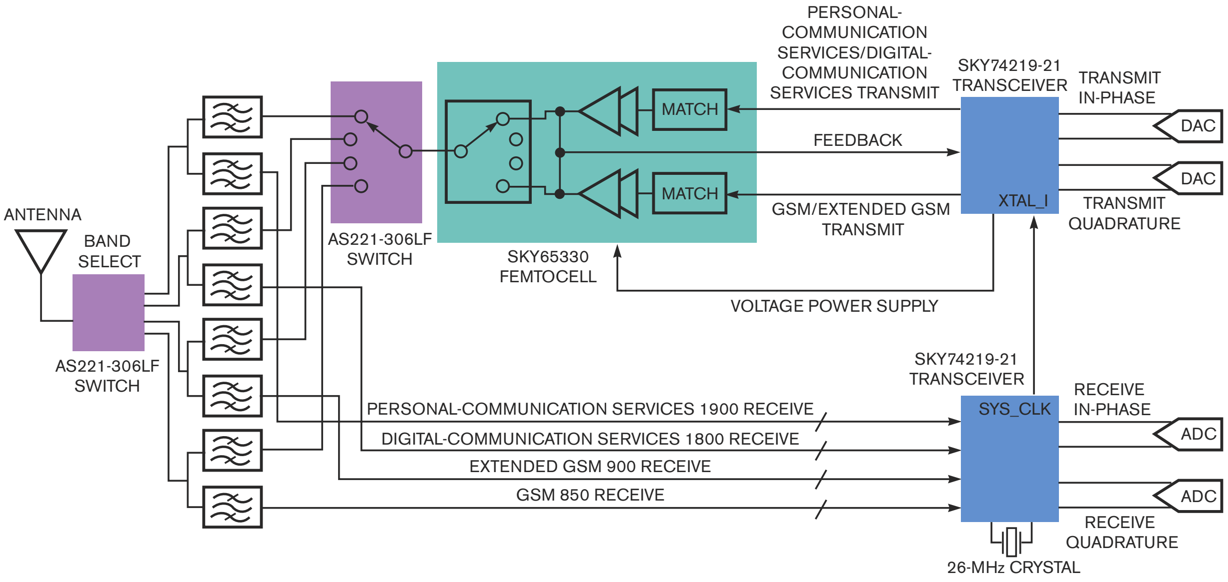


Figure 2 Operators are focusing on next-generation cell-base-station technology, such as femtocells, that goes beyond 3G (courtesy Skyworks Solutions).

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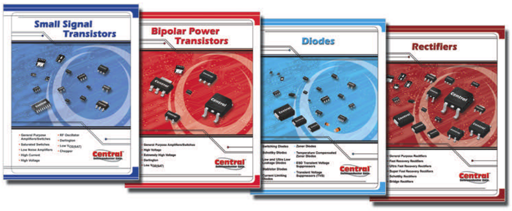

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separate radio structured mesh network with intelligent nodes and dynamic channel management, says Francis daCosta, founder and chief technology officer of Mesh Dynamics. "The regular 2.4-MHz Wi-Fi band can get pretty crowded," he says. "The 5.8-MHz band or any other used solely for this purpose can act like a diamond lane that removes a lot of frequency-interference and congestion issues." In highly congested areas, even if a carrier offloads only some of the data to a complementary network before it hits cell towers, it will improve cell service for all (**Figure 3**). Municipal Wi-Fi failed for multiple reasons, but commercial mesh networks remove one of its main obstacles, which was competition with cell carriers (**Reference 3**). "Carriers can put down a Wi-Fi node where needed, it's unobtrusive, and there's no licensing involved," says daCosta. Dual-mode-cell/Wi-Fi terminals that can take advantage of this situation, such as the iPhone, are becoming more common.

"In networks built from scratch, a key element of the business plan is the high cost of the backhaul," says John Baker, vice president of technical marketing for Andrew's wireless-networks-solutions group. Primarily in locations without land-line connections, carriers are deploying microwave-backhaul networks. "Of course, you can also use IP over land lines or over microwave, but, even though its benefits [offer] higher bandwidth and [the lowest] cost, there are timing challenges with synchronizing base stations to the core of the net," he says.

SILICON ISSUES

Many silicon vendors are now offering front-end silicon for WiMax, as well as other access technologies. These chips include RF stages, mixers, ADCs, DACs, and digital filtering. Others are offering baseband SOCs (systems on chips) or embedded multicore processors. Wireless-networking-equipment manufacturers are leveraging multicore chips to create equipment that can keep up with the vast amounts of data that 3G and other

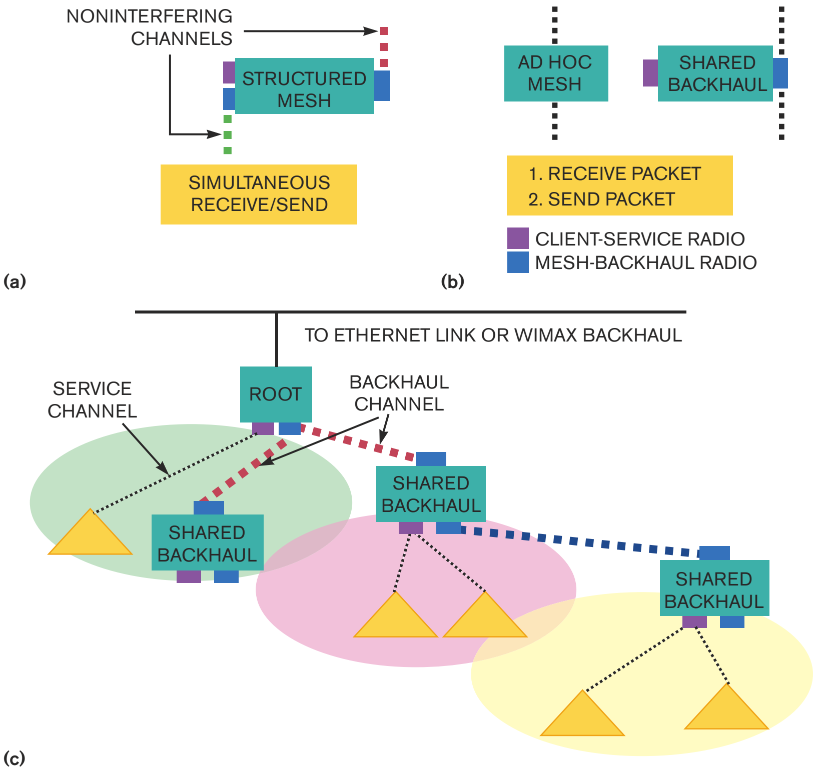

Figure 3 You can build a separate radio structured mesh network with intelligent nodes and dynamic channel management (a) as an alternative to a radio mesh backhaul (b). The result is a network in which service and backhaul channels are both dynamically reallocated to minimize channel-interference effects. Locally changing the backhaul channels has no effect on the rest of the network (c) (courtesy Mesh Dynamics).

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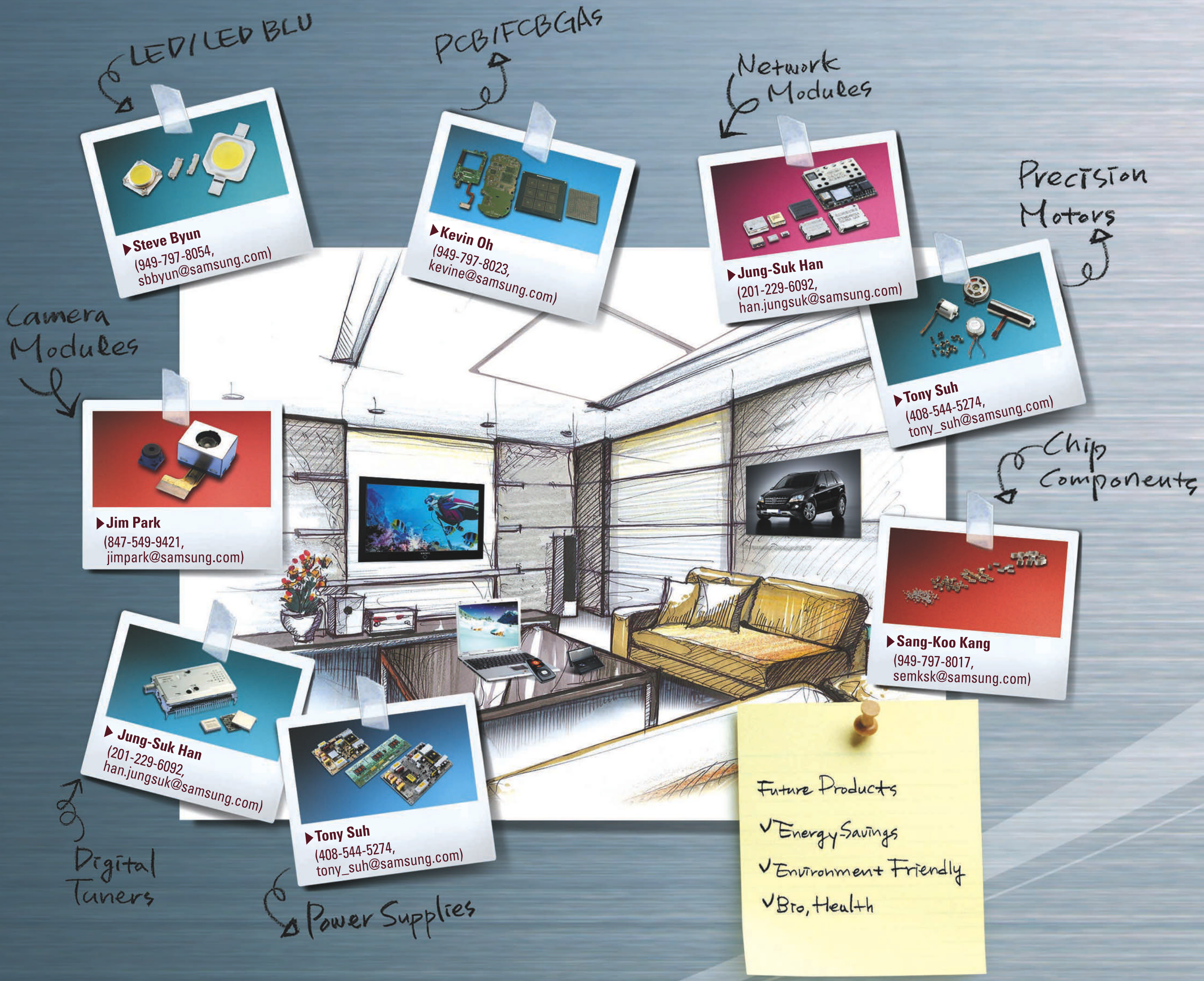

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technologies require, says Stephen Turnbull, high-performance-embedded-processor-portfolio manager for Freescale Semiconductor.

Designers of several major base stations for 3G W-CDMA networks are using multicore DSPs, says Ramesh Kumar, manager of wireless-base-station-infrastructure products for Texas Instruments' communications-infrastructure group. As cost pressures rise on 3G networks because of their expansion into developing markets, multicore chips can help increase channel-card densities and maintain relatively lower cost and power consumption. "In the past, each channel card performed L1/L2 processing for one cell, or base station," he says. "Now, we're looking at three cells per card, moving to six per card within the next three to four years."

Yet, the cost of cell sites has stayed about the same, in part because the electronics cost has come down year over year. "Electronics are becoming less of a percentage of base-station cost because of increased integration and terrific volume growth," says Andrew's Baker.

By the end of this year, Intel's Centrino 2 mobile processors will offer optional support for not only Wi-Fi but also WiMax through a combined Wi-Fi/WiMax module, enabling the development of additional dual-mode PCs and other mobile devices. "We expect that customers may elect to use dual-mode devices for the coverage and service of [3G] EVDO (evolution data optimized) and the added boost of WiMax in metro areas, where it is available," says Kathy Walker, Sprint's chief information and network officer.EDN

⊞ Find an analysis and predictions of how WiMax-mobile-broadband-data services might fit with short-range Wi-Fi networks and 3 and 4G wireless WANs in "WiMax gains in mobile-broadband game, but 4G lurks" at www.edn.com/article/CA6426878.

⊞ For a look at how 3 and 4G networks will likely handle mobile TV and video, see "Mobile television: strong, weak, or zero reception?" at www.edn.com/article/CA6526814.

⊞ For a discussion of the ramifications of 4G networks for handset-silicon architectures, go to "4G wireless: evolution or watershed in SOC architectures?" at www.edn.com/article/CA6486025.

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AUTHOR'S BIOGRAPHY

Contributing Technical Editor Ann R Thryft has been writing about technology, including wired and wireless networking, for more than 20 years. You can reach her at athryft@earthlink.net.

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BY GORDON WILKINSON, PhD • TRINITY CONVERGENCE

Designing intelligence into door-entry and security systems

DESIGNERS NOW HAVE GREATER OPPORTUNITY THAN EVER BEFORE TO DESIGN MORE INTELLIGENCE AND FLEXIBILITY INTO PERSONAL-SECURITY SYSTEMS BY USING MATURE AND PROVEN STANDARDS-BASED TECHNOLOGY. LEARN ABOUT SOME OF THE KEY CHALLENGES TO IMPLEMENTING HIGH-QUALITY, COST-EFFECTIVE, AND SECURE DOOR-ENTRY AND VIDEO-MONITORING SYSTEMS USING IP VOICE AND VIDEO TECHNOLOGY.

Personal security at home, on the street, or in a military setting is a permanent and growing concern; as a result, the products and technologies that address this security continue to see rapid market growth. A significant part of this market uses IP (Internet Protocol) video-surveillance systems—from extensive camera installations in metropolitan areas to small businesses and residences. Although this article refers to "door-entry systems," keep in mind that you can apply this technology to many markets—video doorbells, video baby monitors, and even military applications. Door-entry and video-surveillance systems have become more realistic propositions at the low end of the market in both deployment and overall cost, mainly because of technological advances that support lower prices. These advances are largely due to both the widespread use of IP-based packet networks and the quality improvements in hardware and software.

Many of today's door-entry and security systems employ analog, point-to-point connections feeding voice, video, or both over relatively short distances using expensive coaxial cabling. The costly addition of switching units to reroute the signals provides some flexibility, but overall flexibility is limited. Packet-based networks, however, provide a high degree of flexibility versus legacy analog systems. IP-based door-entry systems now enable viewers to observe images from any number of surveillance cameras that connect to their networks. They also now provide IP-based voice- and video-intercom capabilities both within and outside a LAN. The door-entry terminals that connect to the Internet can double as access points, so that service providers can use them for browsing or revenue-generating services. Today's IP-based door-entry systems can also manually record video or record when certain events trigger the equipment and can route this recorded video for storage at any point on the network. Some of these security systems also provide a "concierge" service that intercepts late-night calls and reroutes them to eliminate disturbance from unwanted visitors. Product design and development of these systems are also efficient because designers can reuse hardware and software for a range of applications and scenarios, such as in apartment complexes and industrial facilities (**Figure 1**).

The key drivers of this technology are the growth of broadband and the trend toward IP networks and IP-based communications. Also consider that you can use the same silicon devices in VOIP (voice over Internet Protocol) and video telephony in door-entry and surveillance systems. This extensibility provides a considerable advantage in reducing per-unit

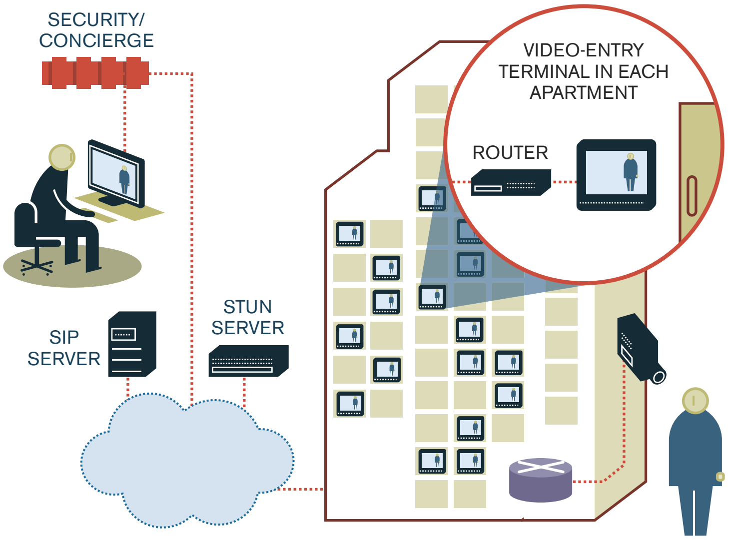

Figure 1 Some IP-based door-entry systems provide a "concierge" service that intercepts late-night calls and reroutes them to eliminate disturbance from unwanted visitors.

costs, as well as the benefit of a solid technological foundation for equipment manufacture and network reliability.

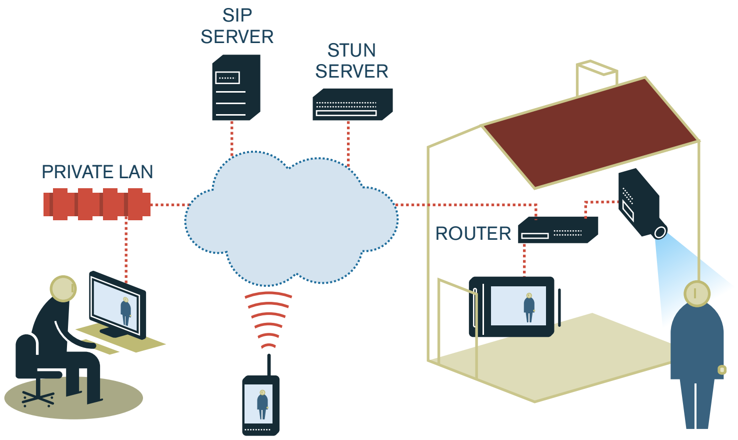

Figure 2 IP networks deliver flexibility to the end user.

ENABLING NEW APPLICATIONS

Perhaps most significant in the rapid growth of the IP-communications revolution and of IP-connected multimedia devices is the trend of embedding more and more "intelligence" at the edge of the telecommunications network. When VOIP services first emerged, media gateways resided in the core of the telecommunications network, which converted the PCM (pulse-code-modulated) voice from the PSTN (public switched-telephone network) into IP packets and vice versa. PBXs (private-branch exchanges) soon adopted the use of this technology in office or apartment buildings, handling comparatively fewer channels. Today, VOIP typically finds use as close to the edge of the network as is possible: at endpoints at which generation or reception of voice and video data occurs, such as within a telephone in the consumer's home. Endpoint devices include cameras, handsets, monitoring stations, and home terminals. The components of the endpoint are the main focus of security-communications-equipment manufacturers. The telephones themselves can now connect to the IP network and make VOIP calls; with the increased bandwidth that broadband lines offer, you can now make V2IP (voice-and-video-over-Internet Protocol) calls from these endpoints and use almost-identical endpoints as intercom units within video-doorbell and -security systems.

This migration to the network's edge and into endpoint devices is largely a result of the industry's acceptance of the SIP (session-initiation protocol) as the signaling and call-setup protocol of choice for IP-based communications. SIP's ability to establish rich, multimedia communication sessions and enable features such as security and network intelligence—that is, "presence"—is lending itself to a host of other applications outside the traditional telecom function.

Figure 2 shows an IP network with the key elements for a variety of V2IP communications, including the endpoint; the SIP-registration server to identify and direct communications sessions between SIP-based devices across an IP network; the STUN (simple-traversal-of-user-datagram-protocol-through-network-address-translator) server, which helps the SIP signaling operate correctly even when the endpoints are behind a NAT (network-address-translation) unit; and the router for routing IP data around the network.

CAN YOU SEE ME NOW?

The endpoint in a video-doorbell or -security system is typically wall- or desk-mounted in an apartment or an office. It comprises a microphone that connects to amplification and analog-to-digital-conversion circuitry, typically within a codec device; an amplified speaker that connects to digital-to-analog-conversion circuitry, typically within the same codec device; an analog or digital Web or surveillance camera; a video display, such as an LCD; an Ethernet or wireless-LAN interface; and a processing device, which includes a CPU with the processing capability for V2IP and any other applications the endpoint requires. A coprocessor within the device handles the video coding. The endpoint also includes V2IP software running on the CPU and in the application layer of the operating system. This software requires audio- and video-media processing and SIP-call control (**Figure 3**).

Most endpoints run some form of embedded operating sys-

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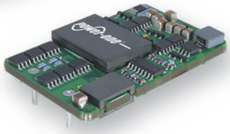

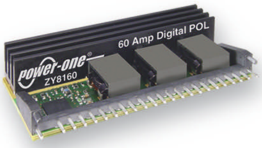

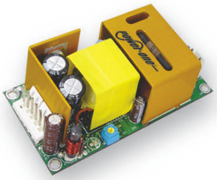

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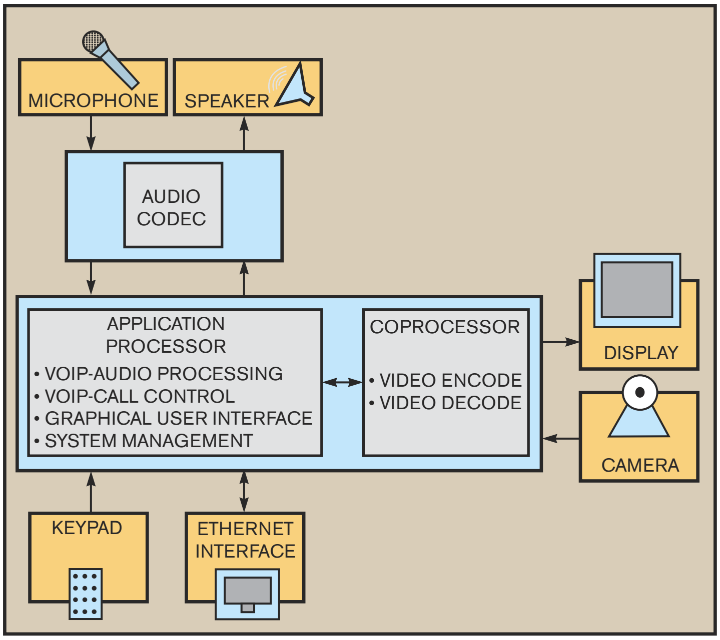


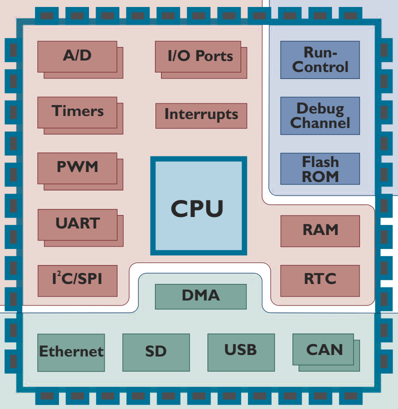
Figure 3 The endpoint in a video-doorbell or -security system comprises a microphone, an amplified speaker, an analog or digital Web or surveillance camera, a video display, an Ethernet or wireless-LAN interface, and a processing device.

tem on the CPU. The operating system can be proprietary, but the consumer-electronics and communication industries tend to use embedded Linux and Win CE. To use Linux or Win CE in an endpoint, a manufacturer creates or licenses a BSP (board-support package) for the CPU, which includes a root-file system with files and directories for applications, drivers, and configuration files; a kernel, which manages the CPU, memory I/O, and other resources; and driver programs for controlling peripherals. The operating system controls its peripherals, such as the audio codec, camera, and video display, through drivers. Linux provides standard interfaces to audio, including OSS (Open Sound System) and ALSA (Advanced Linux Sound Architecture), and video, including V4L2 (Video for Linux 2), to ease portability between devices, and many manufacturers of peripherals provide free Linux drivers with their products.

Many silicon vendors provide reference platforms for their processing device, which customers can use to help accelerate their endpoint-hardware design. These platforms usually include most of the peripherals for the design of an endpoint, along with manufacturing information. They also typically include a BSP in source code, so that designers can use the reference platform as a starting point for software and hardware development.

Before a call can take place, you must be able to set up a connection between two endpoints, such as two intercoms within an apartment building. For small networks, you can make connections using the IP addresses alone or using a proprietary signaling protocol. However, for large networks, particularly when the two endpoints connect over the Internet, for example, it is better to use SIP because it intelligently handles the negotiations to securely and reliably establish these communications.

A SIP endpoint must first make itself known to a SIP-registration server, which is a means of discovering and identifying other SIP users in the network. The SIP user has an identification that uses the same format as an e-mail address—sipuser@sipservice.com, for example, in which "sipservice" is a SIP-network provider. If one SIP user wishes to call another SIP user, the first SIP user sends an invitation that indicates the IP address to which the second user should direct media. The invitation should also indicate the capabilities of the endpoint, such as which audio and video codecs it supports. The SIP server directs the invitation to the remote endpoint using a look-up service. The remote endpoint then responds directly to the initiating endpoint with its own capabilities and contact details. After



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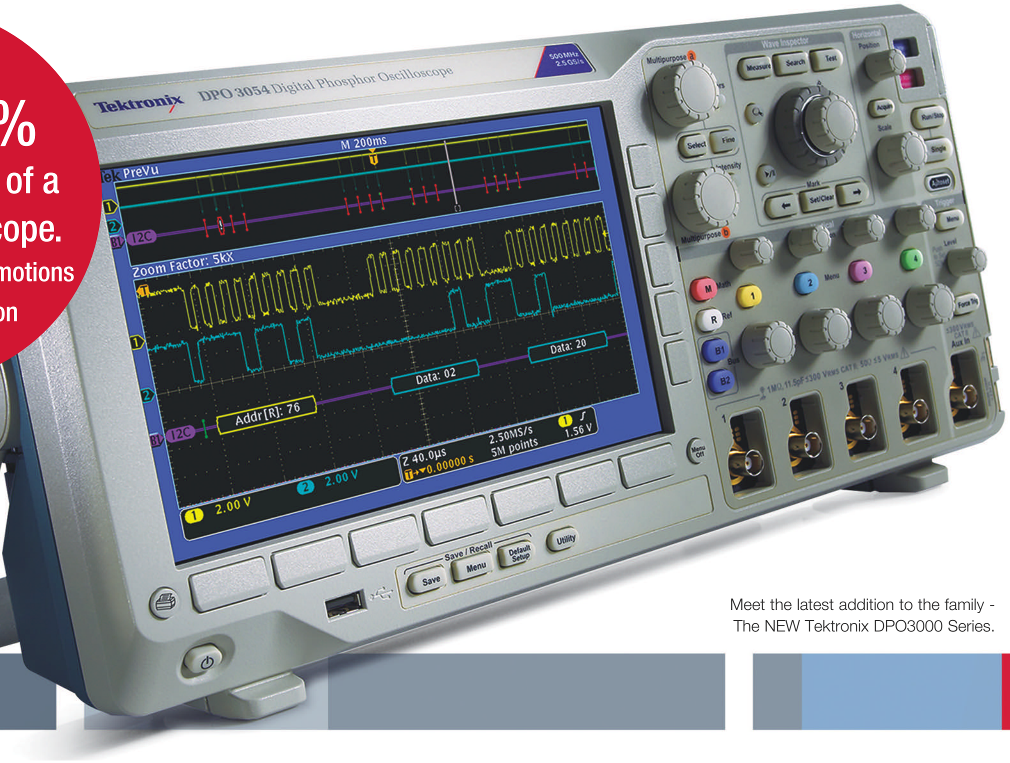

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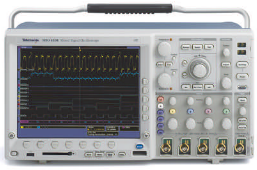

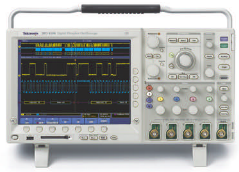

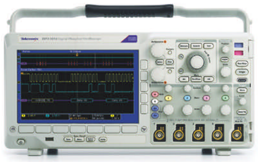

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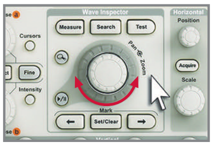
Serial Bus Trigger and Decode	I^{2}C, SPI, RS-232/422/485/UART, CAN, LIN



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these negotiations are complete, the call commences with voice and video communication.

Apart from simple connection of two parties, SIP offers other enhanced services, such as call forwarding, call hold, voice mail, and instant messaging. A voice and video call, such as one that a video doorbell would set up, comprises one audio stream and one video stream. These streams are separate in the network and much of the software they use, but you must combine and synchronize them at the endpoint to ensure a good user experience. In both cases, the data streams pass through similar processing networks.

The encoding path from the microphone and the camera to the network includes the audio/video driver, which receives sampled speech and video from a buffer that a codec device feeds. After this process, AEC (acoustic-echo cancellation) occurs. AEC supports full-duplex, hands-free, speakerphone capability, which requires tuning to the device's acoustic properties. After AEC, video preprocessing occurs. During this step, the video stream may require resizing, rotation, or mirroring. Next, a speech- and video-coding process compresses the sampled data stream to reduce bandwidth requirements within the network. The bandwidth available is one factor in determining the codec and the video-image size. A common speech codec is G.729; H.264 is now in demand for video.

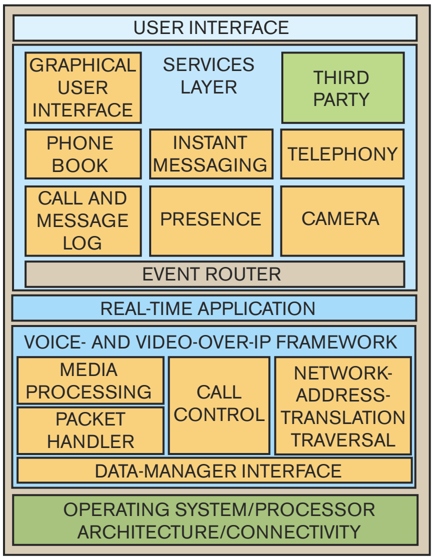

Figure 4 A framework that handles the lower levels of a VOIP and video-over-IP module consists of separate modules, each focusing on individual tasks.

After this process, packetization segments the data stream into blocks for traversal of the network. Each of these requires an RTP (real-time-protocol) header to help with reconstruction of the stream at the remote end. The RTP header includes fields such as sequence number, time stamp, and SSRC (simple server-redundancy protocol), a number unique to the stream. UDP (user-datagram-protocol) and IP processing occurs next. In this step, the RTP packets pass to the IP stack and receive a UDP header corresponding to the destination address they arrived at during the signaling process.

After encoding, the decoding process takes place. Decoding operates on the data stream it received from the IP

network. First, during UDP and IP processing, received media packets pass through the device's UDP/IP stack. A jitter buffer assembles the received packets, using the RTP-header information, before decoding. The management of this buffer handles out-of-order and lost packets using PLC (packet-loss-concealment) techniques and is key to the device's QOS (quality of service). During audio and video decoding, the compressed data decodes to a raw format before passing on to the audio and video drivers.

FUNDAMENTAL BUILDING BLOCKS

For the endpoint to function correctly in real time, these individual functions must take place in the correct sequence; all must coexist in the same processing device such that you can consider them as a single VOIP and video-over-IP module operating alongside any other applications the device requires. The V2IP module must be configurable in many ways, such as its management of drivers, to allow for low-power modes or for interaction with higher layers of the system, such as calls directly from an address book.

The best way to achieve these objectives is to provide a framework that will handle the lower levels of a VOIP and video-over-IP module. This framework consists of separate modules, each focusing on individual tasks (**Figure 4**). The objective of the framework is to speed the overall product design and development. A real-time application manages the modules in the framework; the application processes at the rate of incoming and outgoing data and determines the behavior of the modules by means of a set of APIs (application-programming interfaces). The use of APIs for interfacing to the underlying framework allows you to abstract the application code from the scheduling of each of the components within each module, but it does have control over key components, such as codec, AEC, frame rate, image size, and bandwidth, to ensure the best user experience for the network conditions.

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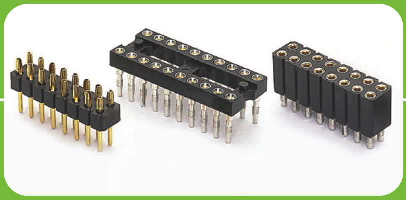
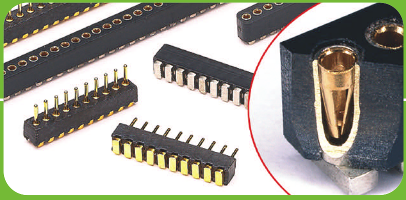
The real-time application responds indirectly to user commands, such as making and answering calls. The user typically makes these commands using a GUI (graphical user interface) that itself has underlying service applications to support a phone book and its database or the logging of calls and messages, for example. The GUI and service applications behave differently from the real-time application in that they are event-driven rather than taking place in real time. For this reason, you must set up a communication path, such as the event router in the **figure**, between the two layers. The event router passes messages between the event-driven and real-time parts of the system. You must use a protocol and provide a queuing mechanism for these messages. You can use third-party-software vendors as sources for ready-made and tested software that provides all the applications from the GUI and services to the real-time application.

IP networks can overcome the connectivity disadvantages of point-to-point analog-door-entry and security systems. These networks can connect many endpoints and use the





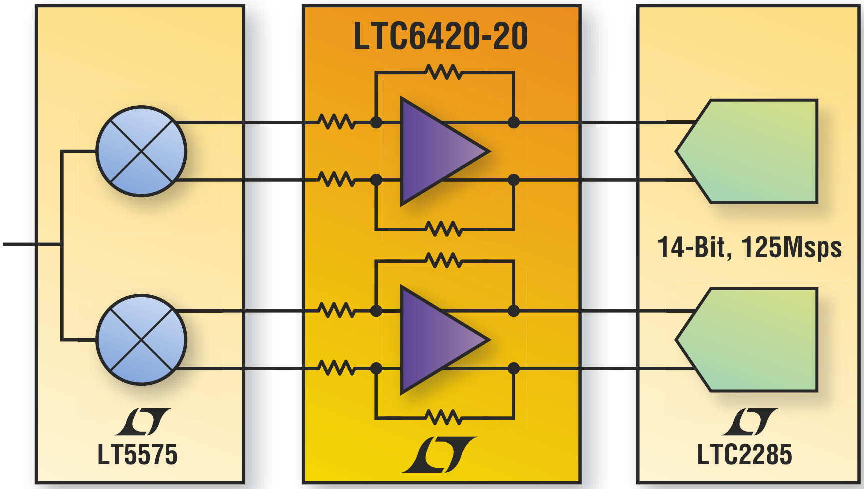
same cabling for both video and audio data, and they can also control those endpoints. However, devices only recently emerged that allow sufficiently high-quality video to traverse these networks at a reasonable cost. These devices are now widely available due to the increasing popularity of VOIP and V2IP with consumers, and, because their functions are almost identical, they can find use within door-entry and security systems. Therefore, despite the fact that IP systems offer so much, their overall costs remain low.

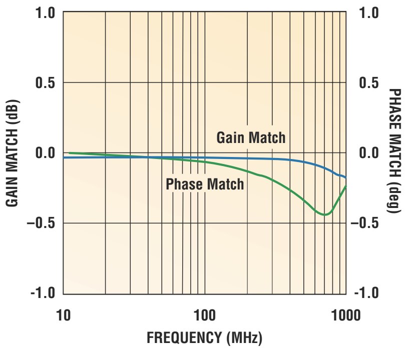
The move from analog to digital packet-switched systems from a technical perspective is not trivial. However, you can gain much by outsourcing elements of the system and working with experienced software suppliers and silicon vendors offering devices targeting this market. A silicon supplier can provide reference designs to speed the hardware design and a BSP to afford a platform for application code. A software supplier can provide a framework with already-written code for the most specialized parts of the V2IP-software development.

Demand a software approach in which highly optimized speech and video codecs, echo cancellation, and call control all combine into a set of structured modules for use within a system developer's application. This step alone will result in shorter product-development cycles and the realization of significant time-to-market advantages.**EDN**

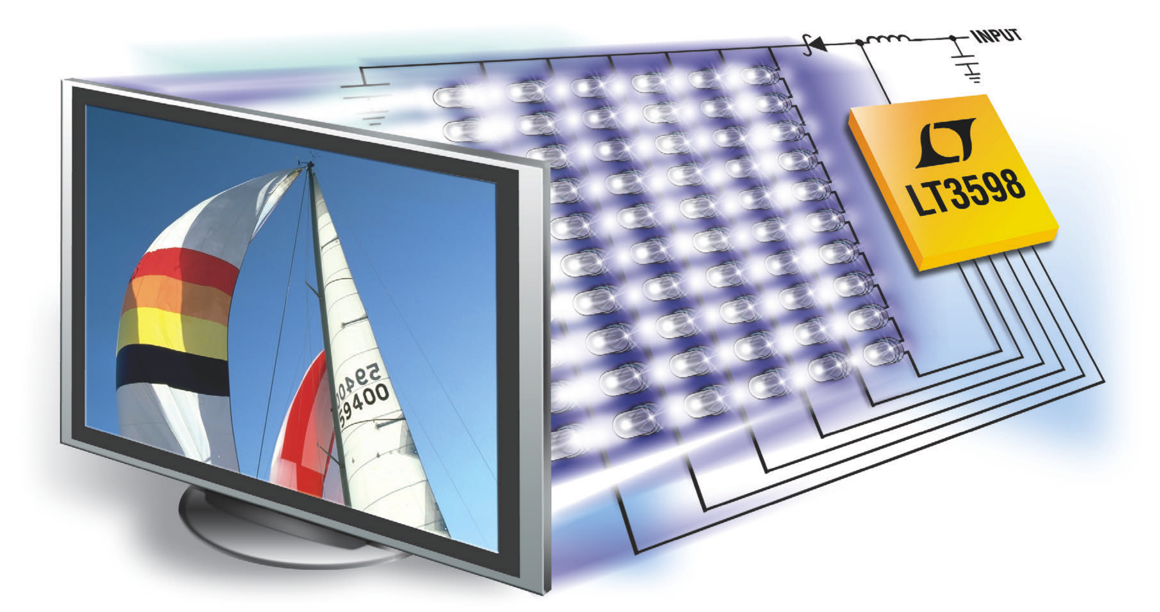
AUTHOR'S BIOGRAPHY

Gordon Wilkinson has worked in the embedded-software and electronics industry for more than 18 years, starting with developing DSP-based instrumentation for nondestructive testing of materials. He then moved on to applications-engineering roles with LSI, Blue Wave Systems, and Motorola, specializing in DSP and VOIP. Wilkinson earned a doctorate in ultrasonic instrumentation and a bachelor's degree in electronics and computer science from Keele University (Keele, Staffordshire, UK). He is now a technical-account manager with Trinity Convergence, a leading VOIP- and V2IP-software developer. You can contact him at gwilkinson@trinityconvergence.com.


LTC6420-20
14-Bit, 125Msps
LT5575
LTC2285


1.0
0.5
0.0
−0.5
-1.0
GAIN MATCH (dB)
1.0
0.5
0.0
−0.5
-1.0
PHASE MATCH (deg)
Gain Match
Phase Match
10
100
1000
FREQUENCY (MHz)

Light Up 60 LEDs



$36V_{IN}$, 2.5MHz, 3000:1 PWM Dimming Range LED Driver

Many small to medium-size panel displays need large numbers of white LEDs for backlighting. Powering and driving up to 16W for these LEDs is challenging due to size and thermal constraints. With the LT®3598 and LT3599, the solution just got easier. These multiple-string LED drivers deliver up to 16W (7W for LT3598) of power and allow a 3000:1 dimming range for brightness adjustment, high LED current accuracy for uniformity of light output, good thermal and LED protection features for a rugged, compact design.

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- LT3599: Drives 4 Strings of LEDs at up to 100mA per String
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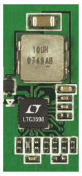
- Adjustable Frequency and Synchronization: 200kHz to 2.5MHz
- Regulated LED Current Even When $V_{IN} > V_{OUT}$
- Programmable LED Temp Derating

LT3598 Demo Circuit



Actual Size

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READERS SOLVE DESIGN PROBLEMS

DIs Inside

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Linear wind-power meter compensates for temperature

W Stephen Woodward, Chapel Hill, NC

The rise of interest in renewable energy created by soaring fossil-fuel costs and global-warming fears has created a matching interest in associated support and demonstration instrumentation. This Design Idea hops on that bandwagon with the ability to directly and conveniently measure an important renewable-energy source: wind power. Handy for quick and easy preliminary evaluation of potential wind-turbine sites, it includes a wind-speed transducer, comprising an optically sensed vane anemometer, and a temperature sensor, comprising a diode-connected transistor. These components interface with a hybrid digital/analog-computation circuit. In combination, they provide a real-time, linear, temperature-compensated readout of wind-power density.

The power-generation potential of wind is $\frac{1}{2}\times$air density (kg/m^3)$\times$air speed (m/sec)^3. To compute it, there-

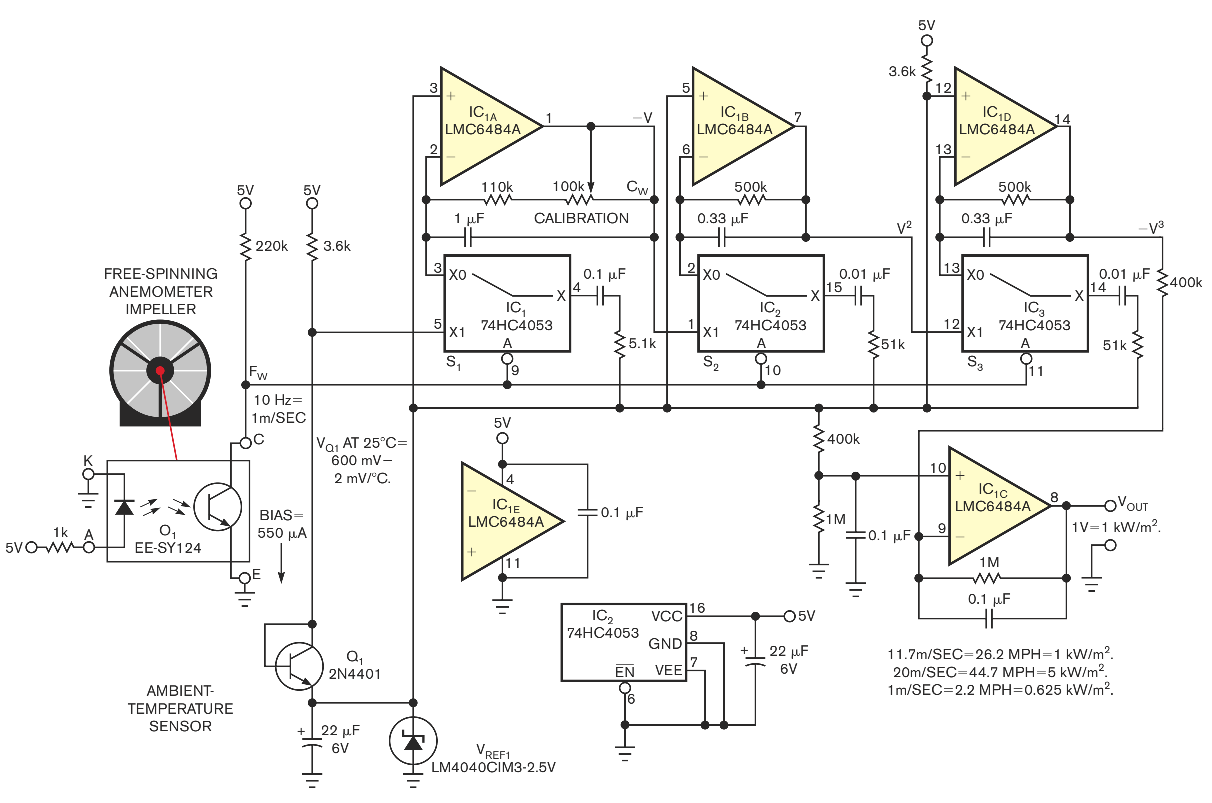

Figure 1 This meter circuit uses a free-spinning anemometer and a diode-connected transistor temperature sensor to measure the available wind power for "green" power generation.

fore, requires estimating air density, which is inversely proportional to absolute temperature; measuring air speed; and calculating a cube.

Here's how the wind-power meter does it. Diode-connected Q_1 has a bias of 550 μA for a 25°C (298K) base-to-emitter voltage of approximately 600 mV and a temperature coefficient of −2 mV/°C. Thus, Q_1 is a voltage reference that tracks the approximate ideal-gas-law temperature dependence of air density: −0.3%/°C. Meanwhile, optical sensor O_1 works with a free-spinning anemometer impeller to produce wind-speed-proportional frequency: $F_W=10$ Hz/m/sec. Conversion of V_{Q1} and F_W into a 1-mV=1W/m² output signal is then the function of the third-order X×Y×Z-multiplying behavior of three cascaded CMOS-switch FVC (frequency-to-voltage-converter) charge pumps: S_1, S_2, and S_3.

FVC S_1/IC_{1A} generates a negative voltage of $-0.17\times V_{Q1}\times F_W$; FVC S_2/IC_{1B} generates $V_2=-V\times F_W=0.17\times V_{Q1}\times F_W{}^2$; and FVC S_3/IC_{1D} generates $-V_3=-0.17\times V_{Q1}\times F_W{}^3$. Finally, differential inverter IC_{1C} shifts and scales $-V_3$ to output $V_{OUT}=0.42\times V_{Q1}\times F_W{}^3=1\text{V/kW/m}^2$.

You can conveniently calibrate the wind-power meter in an automobile being driven on a windless day at a constant speed of 18.6m/sec=41.5 mph=66.8 kph. With the anemometer exposed to the external slipstream, adjust the calibration trimming potentiometer for an output voltage of 4V or, for better accuracy, to the voltage that the following formula that accommodates true air density yields: $V_{OUT}=1.14\text{V}\times$air-pressure millibar/(273+ambient temperature Celsius).**EDN**

Oscillator uses dual-output current-controlled conveyors

Abhirup Lahiri, Netaji Subhas Institute of Technology, New Delhi, India

In the last decade, engineers have done much work in designing and implementing current-mode circuits using second-generation current conveyors, which have higher signal bandwidth, greater linearity, larger dynamic range, simpler circuitry, and lower power consumption than their predecessors. Recently, a second-generation dual-output, current-controlled conveyor has emerged. The device is an active building block (**Figure 1**), and the following equations characterize it: $I_Y=0$, $V_X=V_Y+I_XR_X$, and $I_{Z+}=I_X$; $I_{Z-}=-I_X$. The parasitic resistance at terminal X is $R_X=(V_T/2I_B)$, where V_T is the thermal voltage and I_B is the bias current of the conveyor that is tunable over several decades.

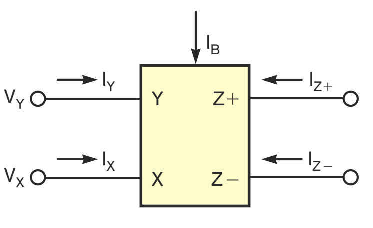

Figure 1 This dual-output current-controlled conveyor illustrates the quantities the equations use.

Figure 2 shows current-controlled oscillators with few components, employing only two dual-output current-controlled conveyors and two grounded capacitors. The devices use no external resistors, and the parasitic resistance at terminal X realizes resistance. The proposed design for the circuit provides electronic controllability of frequency of oscillation.

The characteristic equation for both of the circuits in **Figure 2** is $s^2C_1C_2R_{X1}R_{X2}+sC_2R_{X1}-sC_1RX_1+1=0$. Satisfying Barkhausen's criteria—that the loop gain is unity or greater and that the feedback signal arriving back at the input is phase-shifted 360°—the required condition for oscillation is $C_1=C_2$, and the frequency of oscillation is $f=1/(2\pi\sqrt{C_1C_2R_{X1}R_{X2}})$.

Assuming that $C_1=C_2=C$ and taking $R_{X1}=R_{X2}=V_T/2I_B$ yield a frequency of oscillation: $f=(I_B/\pi CV_T)$. Clearly, the dc-bias current, I_B, can vary the frequency of the current conveyors, and the frequency is, therefore, electronically controllable.**EDN**

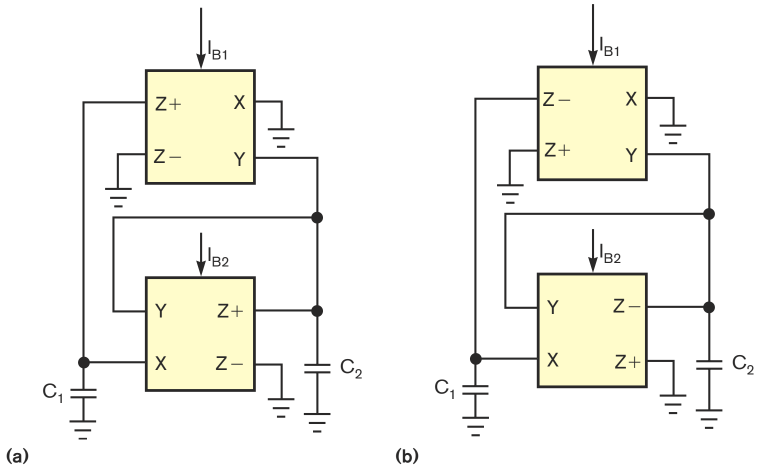

Figure 2 Varying the bias current, I_B, of the dual-output current-controlled conveyor (a) controls its frequency of oscillation versus another device (b).

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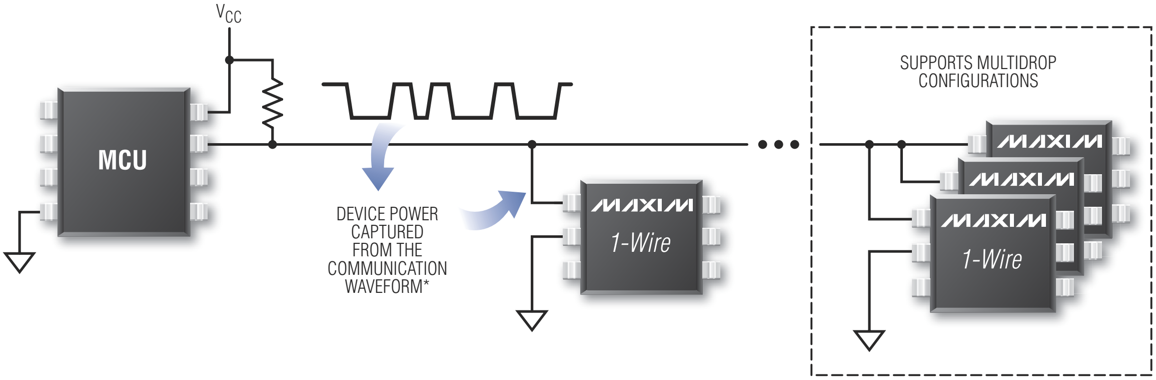

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Temperature measurement	**DS28EA00**: ±0.5°C accurate digital temp sensor
OTP EPROM	**DS2502**: 1kb EPROM
General-purpose I/O	**DS2413**: 2-channel switch with 28V/20mA GPIO
Unique 64-bit serial number	**DS2401**: 64-bit ROM serial number
Real-time clock	**DS2417**: 32-bit RTC counter

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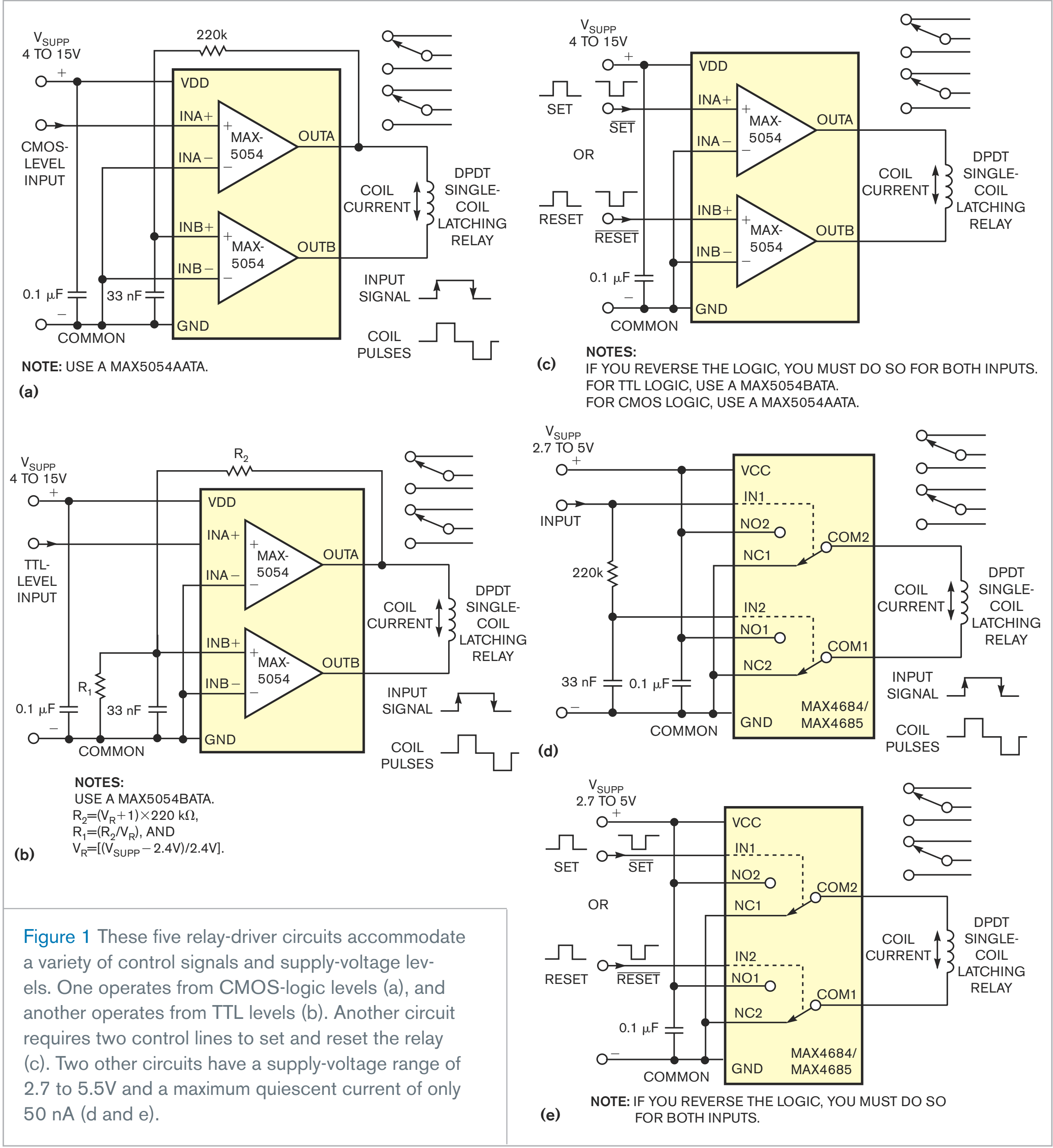
Circuits drive single-coil latching relays

Alfredo H Saab and Tina Alikahi,
Maxim Integrated Products, Sunnyvale, CA

A single-coil latching relay is a relay with memory, usually with a magnetic structure that provides two stable positions for the armature that holds the movable contacts. A permanent magnet provides the force holding the armature in these stable positions. An application of electrical current to the relay coil moves the armature from one position to the other, which in turn changes the contact positions.

Applying to the coil a current pulse in one direction, of longer duration than the specified minimum for that relay type, sets the relay to the first of two stable positions, and it remains in that position after the current ceases to circulate. Current in the opposite direction resets the relay to the other position, which is also stable with no current. The relay then indefinitely remains in that position until a new current pulse toggles it to the other position.



NOTE: USE A MAX5054AATA.

(a)

NOTES:
USE A MAX5054BATA.
$R_2=(V_R+1)\times 220\ k\Omega$,
$R_1=(R_2/V_R)$, AND
$V_R=[(V_{SUPP}-2.4V)/2.4V]$.

(b)

(c)

NOTES:
IF YOU REVERSE THE LOGIC, YOU MUST DO SO FOR BOTH INPUTS.
FOR TTL LOGIC, USE A MAX5054BATA.
FOR CMOS LOGIC, USE A MAX5054AATA.

(d)

(e)

NOTE: IF YOU REVERSE THE LOGIC, YOU MUST DO SO FOR BOTH INPUTS.

Figure 1 These five relay-driver circuits accommodate a variety of control signals and supply-voltage levels. One operates from CMOS-logic levels (a), and another operates from TTL levels (b). Another circuit requires two control lines to set and reset the relay (c). Two other circuits have a supply-voltage range of 2.7 to 5.5V and a maximum quiescent current of only 50 nA (d and e).

DESIGN NOTES

Single-Ended to Differential Amplifier Design Tips – Design Note 454

Philip Karantzalis and Tim Regan

Introduction

A fully differential amplifier is often used to convert a single-ended signal to a differential signal, a design which requires three significant considerations: the impedance of the single-ended source must match the single-ended impedance of the differential amplifier, the amplifier's inputs must remain within the common mode voltage limits and the input signal must be level shifted to a signal that is centered at the desired output common mode voltage.

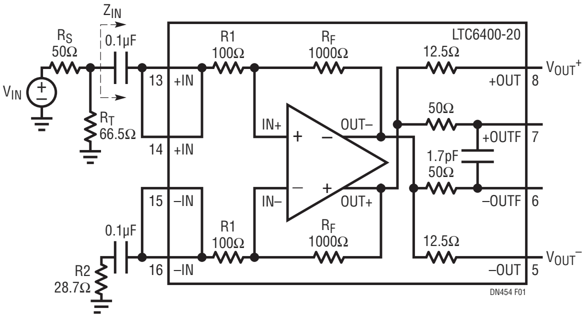
In all cases, input impedance matching to the source impedance is necessary to prevent high frequency reflections. In designs where the single-ended source is DC coupled to a single supply differential amplifier, then level shifting and the common mode limits are also important considerations. The interaction of these three design parameters is non-trivial—component selection requires spreadsheet analysis using the equations described here.

Input Impedance Matching

If input AC coupling is used, then impedance matching is the only design issue. Figure 1 shows an example of a circuit matching a 50Ω single-ended source to an AC-coupled LTC®6400-20 differential amplifier with a gain of 20dB set by internal resistors.

The 66.5Ω resistor, R_T, in parallel with the +IN input impedance, Z_{IN}, matches the circuit input impedance to the 50Ω source. Differential balance is provided with the addition of the 28.7Ω resistor at the –IN input, R2. The balancing resistor assures equivalent feedback factors at the inputs, thus preventing large DC offsets.

To calculate the external resistor values, start by calculating Z_{IN}. Then calculate R_T for impedance matching and the value of the R2 for differential balance. The overall single-ended to differential gain (GAIN) must take into account the input attenuation of the R_S and R_T resistive divider and the effect of adding R2. In this example, the overall gain of the amplifier from signal source to differential output is only 4.44 even though the amplifier has a fixed gain of 10.



$$Z_{IN}=\frac{\sqrt{\left(R_F{}^2\bullet\left(4\bullet R1^2+R_S{}^2\right)+8\bullet R_F\bullet R1^3+4\bullet R1^4\right)}+R_F\bullet\left(R1+R_S\right)+2\bullet R1\bullet\left(R1+R_S\right)}{2\bullet\left(R_F+2\bullet R1+R_S\right)}$$

$$R_T=\frac{R_S\bullet Z_{IN}}{Z_{IN}-R_S}\qquad R2=\frac{R_S\bullet R_T}{R_S+R_T}$$

$$GAIN=\frac{V_{OUT}{}^+-V_{OUT}{}^-}{V_{IN}}=\frac{\left(R1+R2+R_F\right)\bullet\left(R1\bullet\left(R_S-R_T\right)+R_S\bullet R_T\right)}{R_S\bullet R_T\bullet\left(R1+R2\right)}$$

Figure 1. Impedance Matching for a Differential Amplifier with Fixed Gain Integrated Resistors

By AC coupling at the input, the amplifier's input common mode voltage is equal to its output common mode voltage and the single-ended signal is automatically level shifted to an output differential signal centered on the output common mode voltage.

If the input common mode voltage is not 0V, and the source cannot deliver the DC current into 116.5Ω (50Ω + 66.5Ω), then it is also necessary to AC couple the 66.5Ω resistor.

The DC Coupled Differential Amplifier

A general purpose, DC coupled, single-ended-to-differential amplifier circuit with source impedance matching and input level shifting is shown in Figure 2. Level shifting is provided by the reference voltage (V_{REF}). If V_{REF} is set to be equal to the input common mode voltage (V_{INCM}) then the single-ended input signal is

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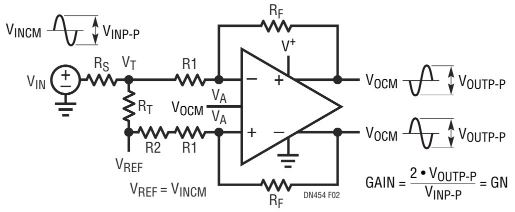

$$R_F = \frac{\sqrt{\left(GN^2 \bullet \left(4 \bullet R1^2 + R_S{}^2\right) + 2 \bullet GN \bullet R1 \bullet \left(2 \bullet R1 - R_S\right) + R1^2\right)} + GN \bullet \left(2 \bullet R1 + R_S\right) - R1}{2}$$

$$R_T = \frac{R_S \bullet \left(R1 + R_F\right)}{R1 + R_F - R_S \bullet \left(GN + 1\right)} \qquad R2 = \frac{R_S \bullet R_T}{R_S + R_T}$$

$$V_A = \frac{R_F \bullet V_{INCM} + \left(V_{OCM} \pm \frac{GN}{2} \bullet V_{INP\text{-}P}\right) \bullet \left(R1 + R2\right)}{R1 + R2 + R_F}$$

$$V_T = \frac{\left(\left(R1 + R_F\right) \bullet \left(R_S + R_T\right)\right) \bullet V_{INCM} + R_S \bullet R_T \bullet V_{OCM}}{R1 \bullet \left(R_S + R_T\right) + R_F \bullet \left(R_S + R_T\right) + R_S \bullet R_T} \pm \frac{V_{INP\text{-}P}}{4}$$

Figure 2. Impedance Matching and Level Shifting for a Differential Amplifer with Gain Set By External Resistors

shifted to a differential signal centered on the output common mode voltage (V_{OCM}).

The design of a single-ended to differential amplifier with external resistors provides an additional design option: specifying the amplifier gain. Figure 2 shows the design equations when the R_F and R1 resistors are selectable, not fixed.

The design of this circuit begins with the value of R1. This resistor must be larger than the input source resistance but not so large as to increase circuit noise. Next, calculate the value of the feedback resistor R_F using the desired gain (GN). Then calculate the value of resistors R_T and R2.

Figure 3 shows an example of a single-ended-to-differential amplifier matching a 75Ω source and level shifting from a 2.5V input common mode to a 1.25V output common mode voltage (typical level shifting required from a 5V single-ended circuit to a 3V differential circuit to drive a high speed ADC). The single-ended-to-differential gain of the Figure 3 amplifier is 2 (the $1V_{P\text{-}P}$ input signal is amplified into a $2V_{P\text{-}P}$ differential output signal, a typical input voltage range of a high speed ADC).

For linear operation, the amplifier's input common mode limits must not be exceeded. Figure 2 shows the calculations for the bias voltage (V_T) of the input T-network (R_S, R_T and R1) and the common mode voltage at the differential amplifier's inputs. For example, in Figure 3, the 1.99V to 2.44V at the amplifier's inputs (as calculated by the V_A equation) is well within the rail-to-rail input common mode range of the LTC6406 (0V to V^+).

Table 1. Sample of LTC High Speed Differential Amplifiers

AMPLIFIER	GBW GHz	SLEW RATE V/µs	VOLTAGE NOISE nV/√Hz	GAIN V/V
LTC6400-26	1.9	6670	1.5	20
LTC6400-20	1.8	4500	2.1	10
LTC6400-14	1.9	4800	2.5	5
LTC6400-8	2.2	3810	3.7	2.5
LTC6401-20	1.3	4500	2.1	10
LTC6401-14	2	3600	2.5	5
LTC6404-1	0.5	450	1.5	R SET
LTC6404-2	0.9	700	1.5	R SET
LTC6405	2.7	690	1.6	R SET
LTC6406	3	630	1.6	R SET

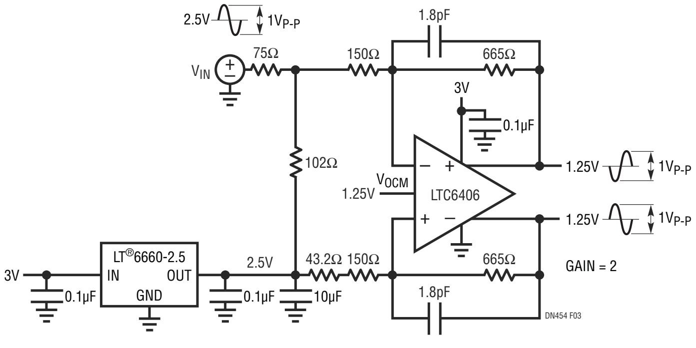

Figure 3. Putting it All Together: A 133MHz Differential Amplifier with External Gain Setting Resistors,Impedance Matching to a 75Ω Source and Level Shifting from 2.5V to 1.25V

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The electronic circuitry to drive one of these relays from logic signals can be a half-bridge if dual supply voltages are available or a full bridge—that is, an H-type power driver—if only a single supply voltage is available. The need to generate reversible-current pulses through the two-terminal coil imposes the use of these bridge topologies. Because the relay itself does not consume power under static conditions, the driving circuitry should also consume minimal power under the same conditions.

Figure 1 illustrates a variety of driving circuits, depending on the input-signal-logic levels, their coding, and the magnitude of the available supply voltages. The circuits in **figures 1a** through **c** drive relays for voltages of 4 to 15V. The circuit in **Figure 1c** requires two separate control lines: The set line sets the relay, and the reset line resets it. You can code the set and reset signals as positive (active high) or negative (active low). You must use the same logic convention for both inputs in this circuit.

The widths of the set and reset signals must be longer than the minimum time required for the relay to operate—typically, 3 to 5 msec. For proper operation, you should apply only one signal at a time; while applying one, the other should remain at the nonactive-logic value. Using positive logic, for example, the signal must go high for 3 to 5 msec, and the other input must remain low until the first signal pulse ends. The choice of IC determines the logic level: TTL (transistor-to-transistor logic) or power-supply-level CMOS (**Figure 1c**).

The circuits in **figures 1a** and **1b** operate from a single on/off-signal line, generating a coil-current pulse with each transition of the input signal. The polarity of the coil-current pulse depends on the polarity of the input-signal transition that generates it (**figures 1a**, **b**, and **d**). The circuit in **Figure 1a** operates from CMOS-logic levels, and the one in **Figure 1b** operates from TTL levels. After each transition, the signal must remain stable for longer than the relay's minimum operating time. The circuits in **figures 1a** and **c** typically draw quiescent currents of 40 µA, and the one in **Figure 1b** typically draws approximately 50 µA. The circuits in figures **1d** and **1e** are similar to those in **figures 1a**, **1b**, and **1c**, but their supply-voltage range is 2.7 to 5.5V, and their maximum quiescent current is only 50 nA.

Because the single-coil latching relay has a memory of its own, you must initialize its position after power-up to a known state, either by exercising the input logic or by analyzing and responding to a signal from the contacts' circuitry. Any of these circuits can deliver as much as several hundred milliamps in either polarity while pulse-driving a relay coil. You can find technical information and data sheets for the ICs in these circuits at www.maxim-ic.com. **EDN**

EDITED BY SUZANNE DEFFREE

supplychain

LINKING DESIGN AND RESOURCES

Consolidation among mobile-IC makers squeezes supply chain

Continuing the considerable consolidation in the mobile-IC supply chain, Freescale Semiconductor (www.freescale.com) announced a planned exit from the cellular-handset-chip-set market. The company in October said that it is exploring its options for the business, including the unit's sale or the formation of a joint venture, just weeks after STMicroelectronics (www.st.com) announced it would buy out NXP's (www.nxp.com) share of its ST-NXP Wireless joint venture. That August-launched company effectively saw NXP end its mobile-IC work. ST then merged in EMP (Ericsson Mobile Platforms, www.ericsson.com/mobileplatforms), creating a formidable competitor to the wireless industry's mobile-semiconductor kingpins, including Qualcomm (www.qualcomm.com).

Analysts believe that, with Freescale's move, more opportunity could open to Qualcomm, however. As part of its action, Freescale updated its mobile-IC arrangement with Motorola (www.motorola.com) whereby Motorola agreed to provide certain consideration in exchange for eliminating Freescale's remaining minimum-purchase commitments.

"In recent reports, we have highlighted the theme of [Qualcomm's] benefiting from rapid consolidation of the wireless-semi industry," wrote Tim Luke, a semiconductor-market analyst at Barclays Capital (www.barcap.com), in a research note.

Freescale is seeking to increase its investments in the automotive and networking markets, as well as in the industrial and consumer markets. "In the cellular-handset-chip-set market, it has become evident that this business needs considerably greater scale … to achieve a position of market leadership and long-term success," says Rich Beyer (**photo**), Freescale's chief executive officer. Freescale's cellular-handset-products business includes baseband processors, RF transceivers, power management/audio, software, and platforms.

GREEN UPDATE

OEMs ANSWER GREENPEACE'S CALL FOR STRICTER REGULATION

OEMs are responding to more-stringent energy requirements from environmental group Greenpeace International (www.greenpeace.org). No governmental organization has mandated the criteria, which include support for global mandatory reduction of GHG (greenhouse-gas) emissions, disclosure of GHG emissions plus emissions from two stages of the supply chain, commitment to reduce GHG emissions with time lines, proportional use of renewable energy in total electricity use of more than 25% operations, and energy efficiency.

"Most of the brands are responding to the more-stringent chemical and e-waste [electronics-waste] criteria," says Iza Kruszewska, toxics campaigner with Greenpeace. She cites Apple, Nokia, Sony Ericsson, and Samsung as top scorers in energy efficiency.

Greenpeace also made note of Fujitsu Siemens Computers (www.fujitsu-siemens.com), which recently set late 2010 as its deadline for eliminating PVC (polyvinyl-chloride) plastic and all BFRs (brominated flame retardants) across its product range. The industry debate about whether the removal of PVC and BFRs from electronics design is the best decision for the environment is still ongoing. Nevertheless, several companies have launched products with restricted amounts of such materials.

OUTLOOK

INDIA, VIETNAM GAINING AS ASIA/PACIFIC SEMICONDUCTOR-SALES GROWTH SLOWS

Gartner Inc (www.gartner.com) has lowered its forecast for 2008 revenue growth in Asia/Pacific's semiconductor market from 6.4% to 5.2%. The research company based the change on the worsening global macroeconomic environment, further eroded consumer confidence, and cloudy visibility in the second half of the year.

Total semiconductor revenue in the region reached \$149.3 billion in 2007 and is forecast to total \$157.1 billion in 2008.

Gartner projects the CAGR (compound-annual-growth rate) of the China/Hong Kong semiconductor market from 2007 through 2012 will be 7.1%. Meanwhile, Gartner expects that India and the countries in the other-Asia/Pacific category, which includes Vietnam, will achieve higher CAGRs of 19.1 and 18.7%, respectively.

India is expected to continue to attract investment from global electronics manufacturers, and Vietnam has become increasingly attractive to global electronic-equipment manufacturers and semiconductor vendors, and "looks likely to emerge as the next major market in the region's electronics industry," Gartner reports.

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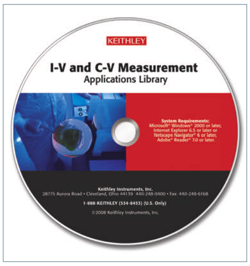

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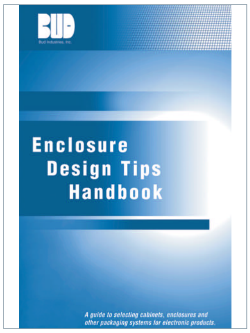

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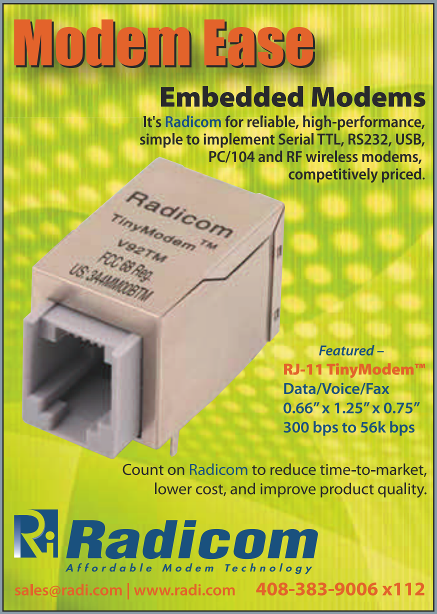

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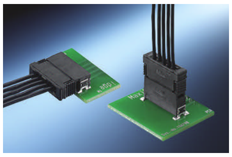
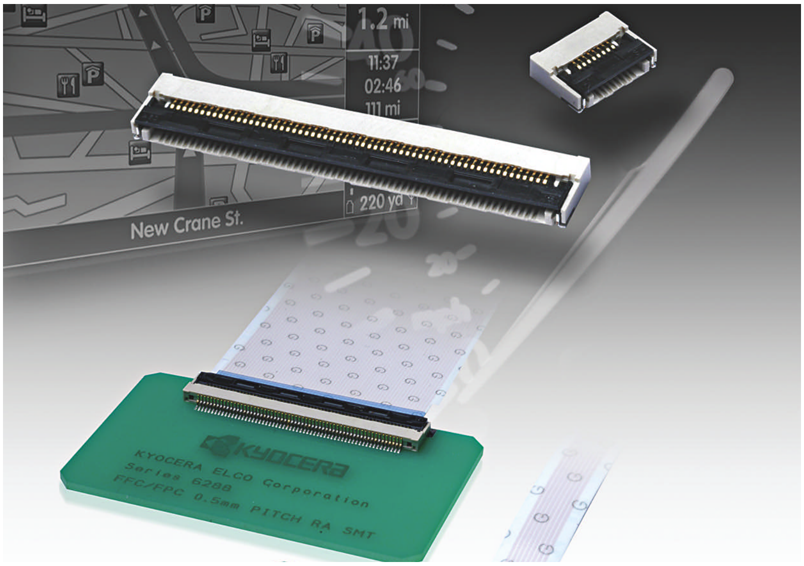


productroundup

CONNECTORS



ZIF-connector series reduces failures from misalignment

The secure-lock ZIF (zero-insertion-force)-6288-connector series features a shaped cable construction providing correct alignment, reducing production-process failures. Providing audible and tactile click feedback allows the device to prevent accidental removal of the cable in the field. The moldings in the connectors accept FFC/FPC cable and lock shapes, suiting audio/visual devices, digital speedometers, tachometers, handheld blood-sugar monitors, and LCD screens. Features include a −40 to +105°C operating temperature and 0.5-mm pitch contacts with a gold-flash finish for higher-reliability soldering. Available in six to 60 positions, the ZIF-6288-connector series costs 40 cents (2000).

AVX Corporation, www.avx.com

End-to-end devices meet TIA/EIA-568-B.2-10-configuration requirements

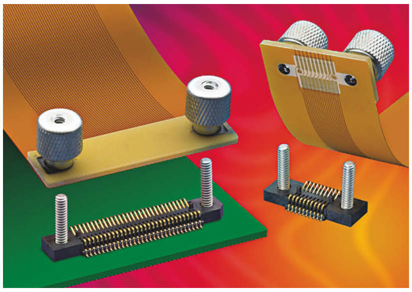
Enabling 10-Gbps connectivity in data centers and structured cabling systems, the ETL-verified Category 6a cabling devices link 10GBaseT networking equipment. Including patch cords, patch panels, keystones, and bulk cabling, the end-to-end products meet all TIA/EIA-568-B.2-10 requirements in channel- and permanent-link configurations, such as alien crosstalk, return loss, insertion loss, propagation delay, and delay skew. The series features bulk cables in 1000-ft reels and aqua, black, and gray options. The keystone units cost $18.99; the bulk cables cost $633 per reel.

Belkin, www.belkin.com

Audio connectors are smaller than XLR connectors

Claiming a 40% reduction in size, compared with standard XLR connectors, the high-density Mini-XL audio-connector series uses one-touch connect/disconnect. The circular device includes ROHS (restriction-of-hazardous-substances) connectors suiting cable and panel-mount applications. A socket insulator minimizes vibration and electrical noise. Features include a disconnect latch lock, gold-plated contacts, and a low-reflectivity satin finish. The series offers a rear housing in plastic or metal for male and female plugs. The Mini-XL plugs are available in three- and six-pin contact arrangements, and prices range from $4 to $6; prices for panel-mount components range from $5 to $7 (500).

ITT Interconnect Solutions, www.ittcannon.com



Wide variety of interface devices have low profiles

The One-Piece Interface suits high-shock/vibration applications with robust design and threaded inserts to mount the connectors to the boards. The dual-row interfaces on the 1-mm-pitch FSI series provides a range of board spacing from 3 to 10 mm. Suiting applications requiring an ultra-low profile, the 1-mm-pitch SEL series features 0.64- and 1.27-mm board spacing, and the SEI series has 1.65-mm board spacing. The high-density GFZ array-interconnect series achieves 1200 I/Os and a 3-mm board-spacing profile. Prices for the One-Piece Interface devices start at 5 cents per pin.

Samtec, www.samtec.com

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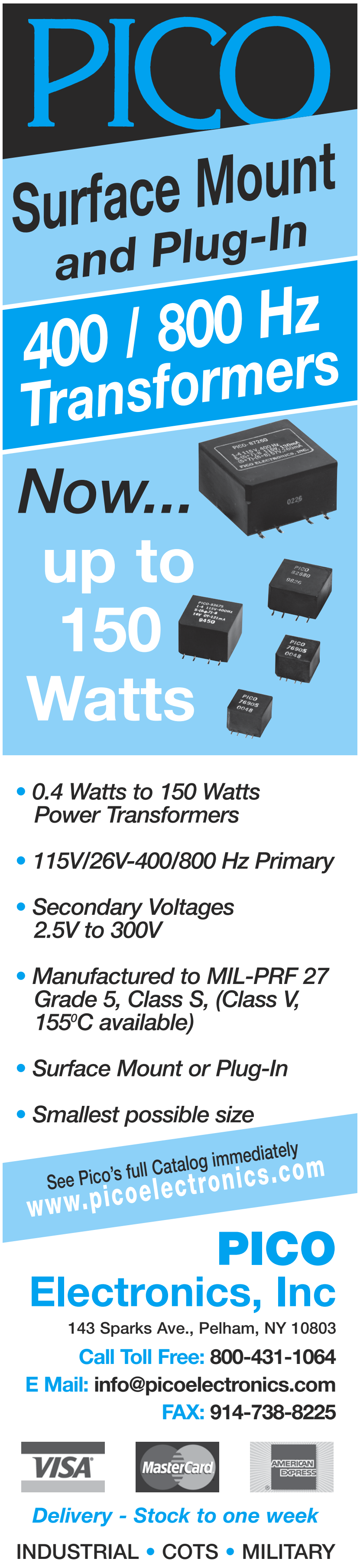

TALES FROM THE CUBE

BY ARNOLD N SIMONSEN • ELECTRICAL ENGINEER

Align up!

DANIEL VASCONCELLOS

A previously published *Tales from the Cube* column (**Reference 1**) brought to memory a similar experience I had with a relay-release time and an attempt to reduce inductive spikes.

As a young engineer in the late ’60s, I was working on the Apollo instrumentation ships, which NASA used to track and communicate with the Apollo lunar-excursion module. The ships had C- and S-band radars, a satellite-com antenna, a telemetry-tracking antenna, a VHF/UHF command-and-control communication antenna, and a large data-processing center. Each of the antennas provided azimuth- and elevation-position-synchro data to a central network.

This network allowed selection of any antenna’s position data for making one antenna act as a slave to another antenna. Large synchro amplifiers drove 23 small synchro amps to amplify the synchro-position data. The 120V, 60-Hz synchro amps required an electromechanical-alignment procedure. The amps could align to approximately 0.1°.

After successful system tests, we noticed that the amplifiers were out of alignment by large amounts—in many cases, 20° or more. Realignments were tedious and time-consuming. We resorted to pinning the shafts to keep them aligned, thinking it was a mechanical problem. Over time, the pins became loose and even bent, however.

The three-wire outputs of the synchros went into a relay-switch network. The relays allowed selection of which antenna would act as a slave. The relay coils each had suppression diodes to reduce inductive spikes, the noise on control lines, and switch-contact arcing. This procedure was standard and accepted.

While monitoring the switching transients, I saw that the relays’ dropout time was a lot longer than their pull-in time. This excess time allowed the outputs of two or more synchro amps to connect across each other during the dropout time of the relay. During switching, the amplifiers also made loud gear noises. This pull-in- and dropout-time difference was new to me, but checking relay characteristics confirmed my observation. Some studying of the use of suppression diodes indicated that diodes would even lengthen the relays’ dropout time. I tried capacitors and RC networks to no avail.

Then, in a diode catalog, I found a Thyrector device from General Electric. It was basically two back-to-back diodes for reducing inductive spikes. I tried using the device to correct the time difference, and it greatly reduced the relays’ dropout time.

My boss was reluctant to make any change because the customer had accepted the system. We had no recording scopes back then, so I set up a fast strip-chart recorder to monitor the relay pull-in and dropout times during typical switching sequences and showed him the two connected amplifier outputs. I repeated the test with the Thyrectors in the circuit, which showed a great reduction of the overlap time and no gear noises during switching. Success!

I replaced the suppression diodes with Thyrectors, and subsequent tests during sea trials showed no synchro-amp misalignments. **EDN**

REFERENCE

1 Lindenbach, Walter, “Time bomb,” *EDN*, Sept 27, 2007, pg 26, www.edn.com/article/CA6479508.

Arnold N Simonsen is an electrical engineer in Tucson, AZ. Like Arnie, you can share your Tales from the Cube and receive $200. Contact edn.editor@reedbusiness.com.

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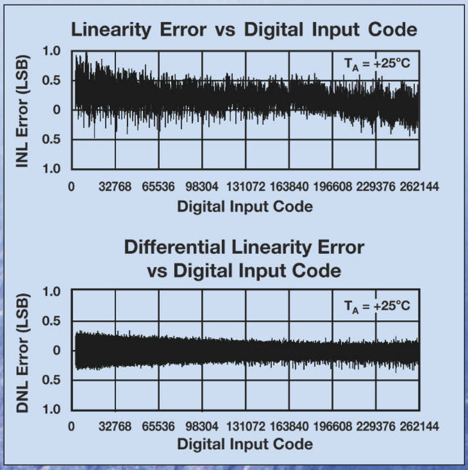
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